

FIG.1

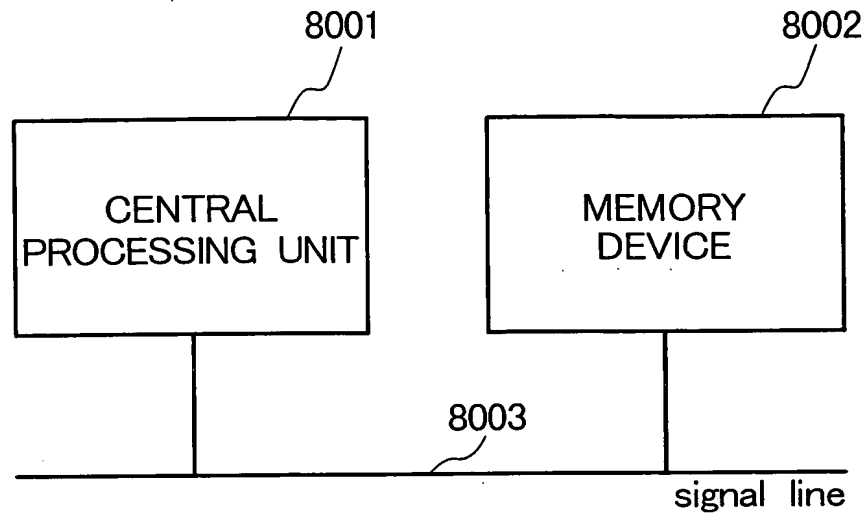


FIG.2

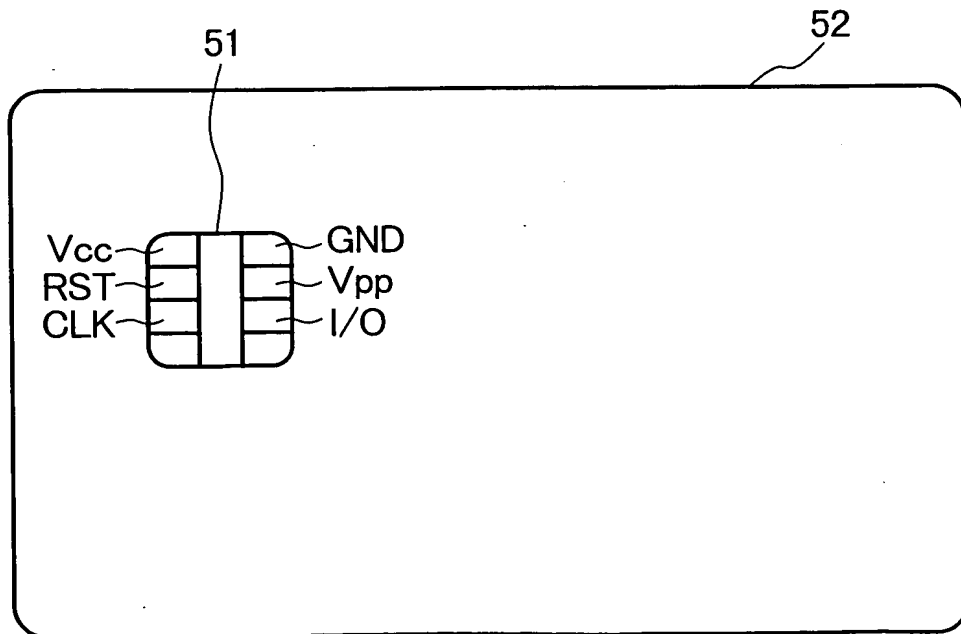


FIG.3

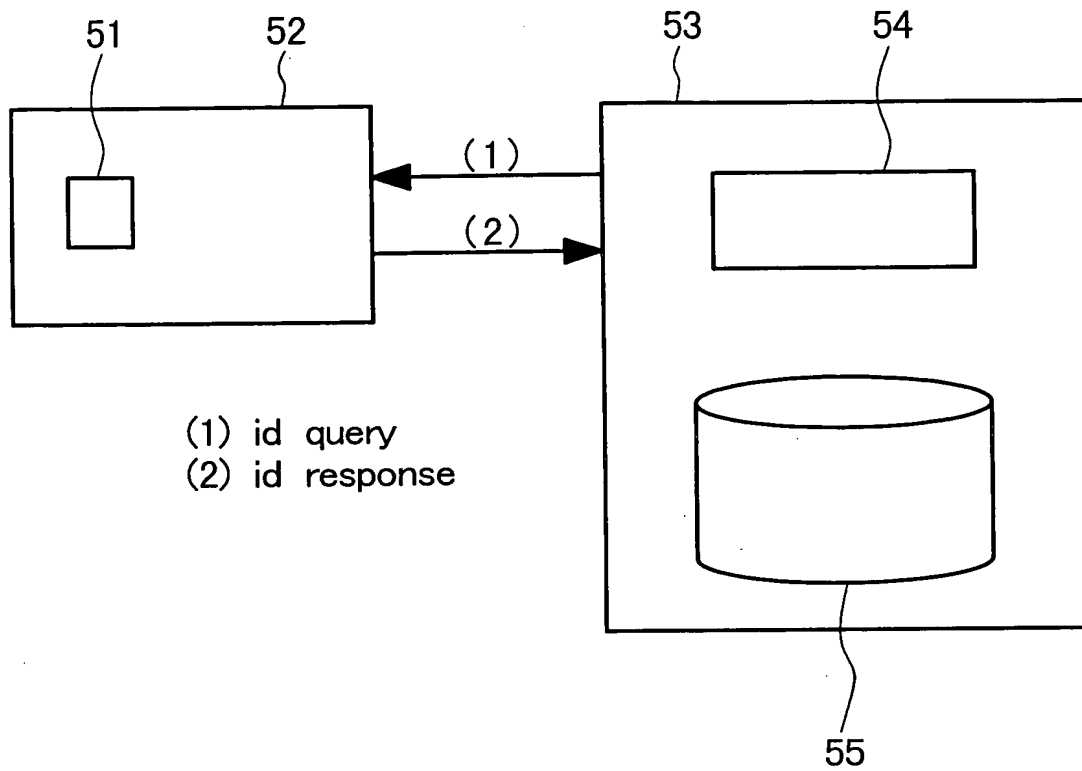


FIG.4

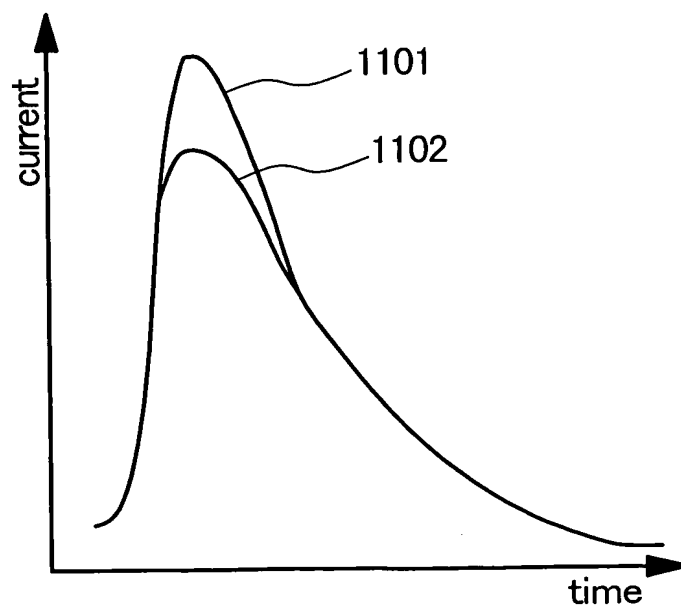


FIG.5

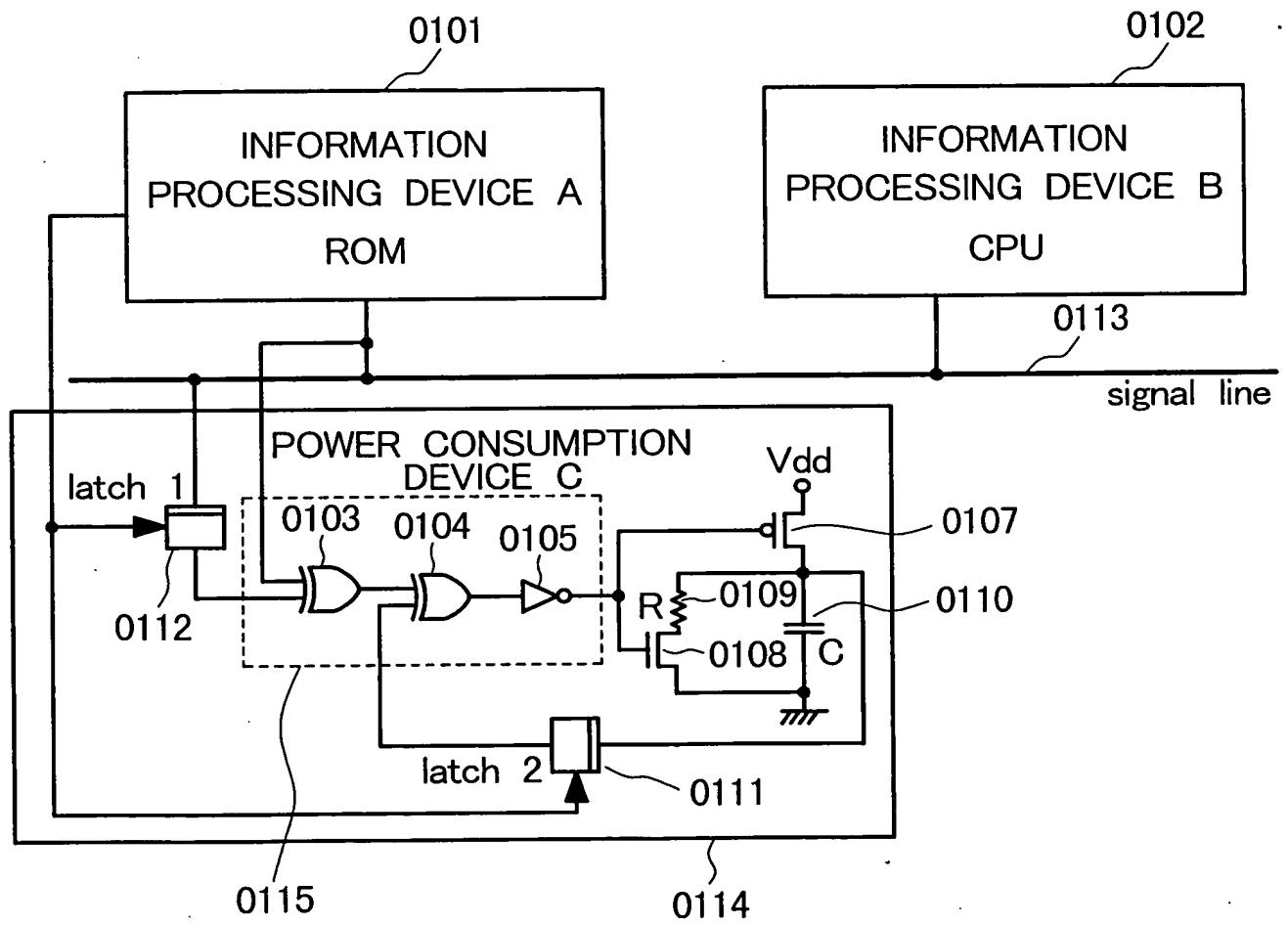


FIG.6

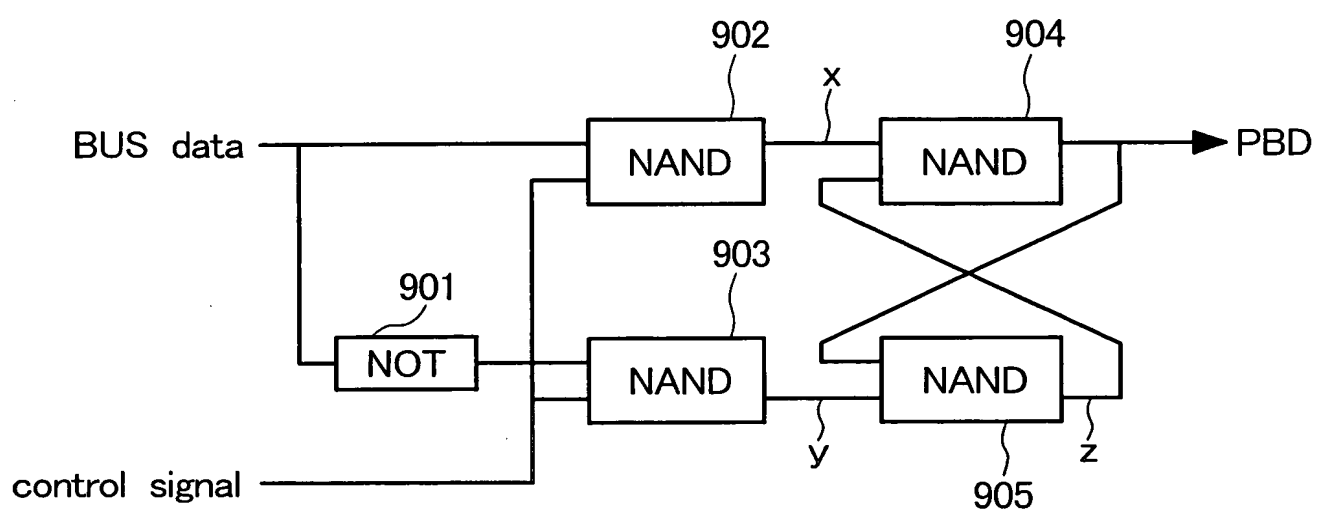
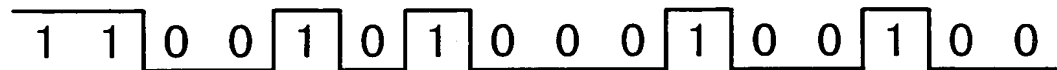


FIG.7A

state of signal line



state of capacitor

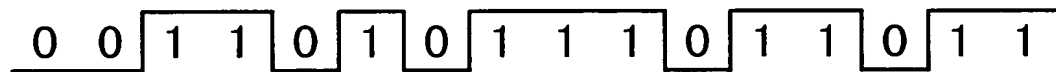


FIG.7B

state of signal line



state of capacitor

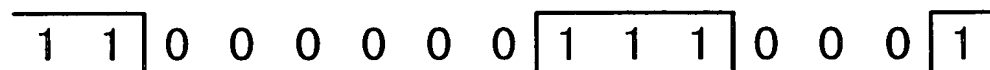


FIG.8

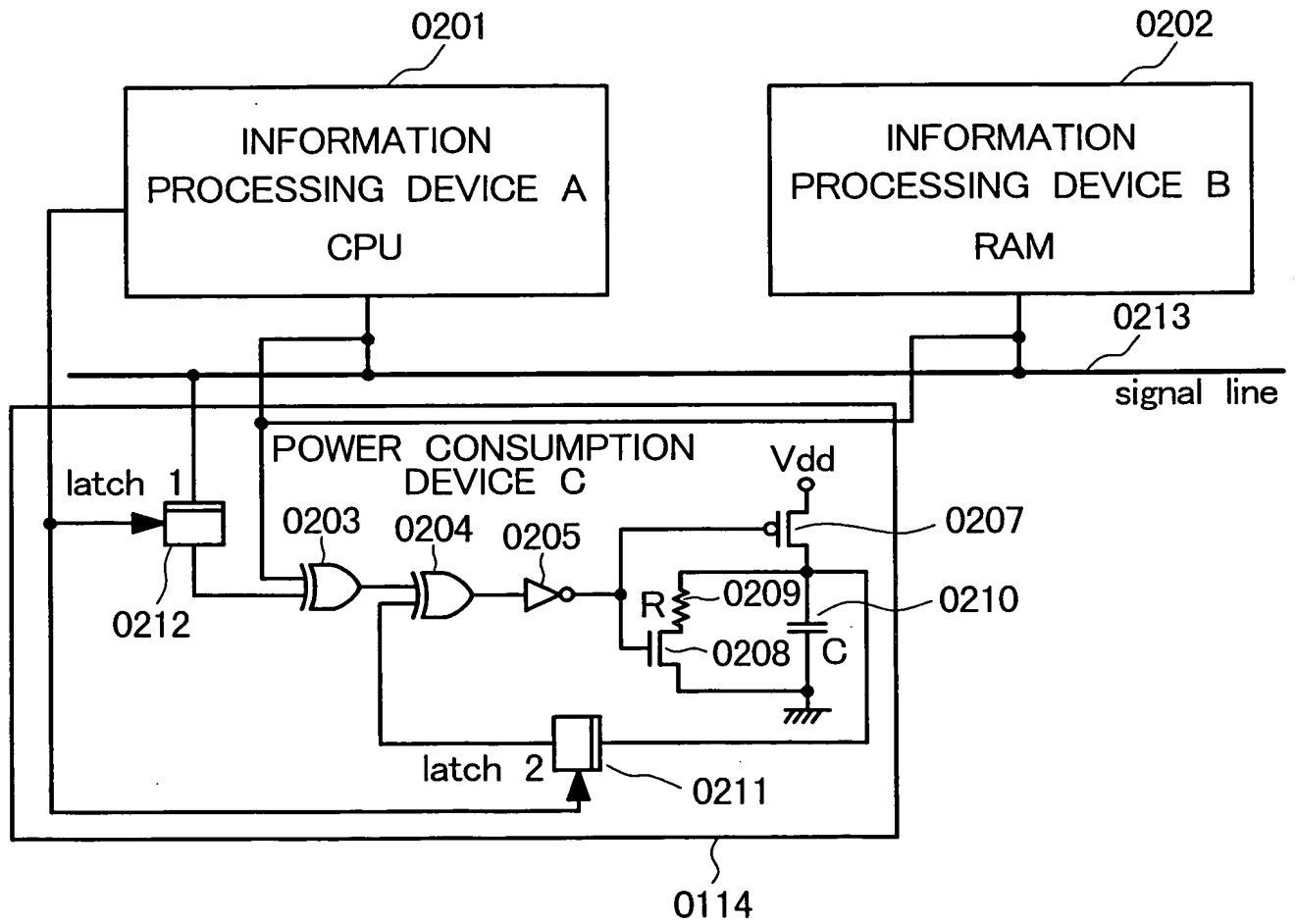


FIG.9

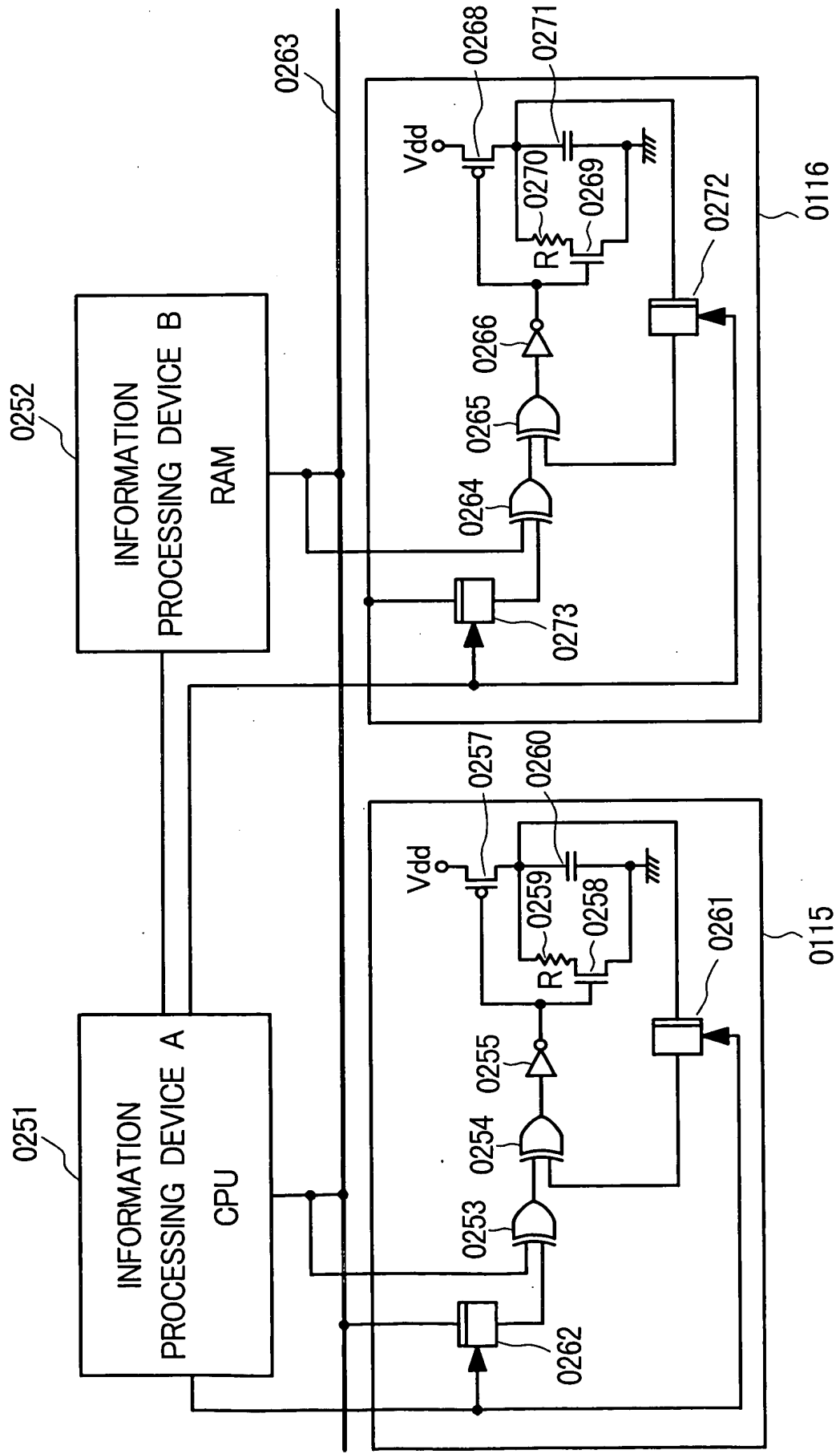


FIG.10

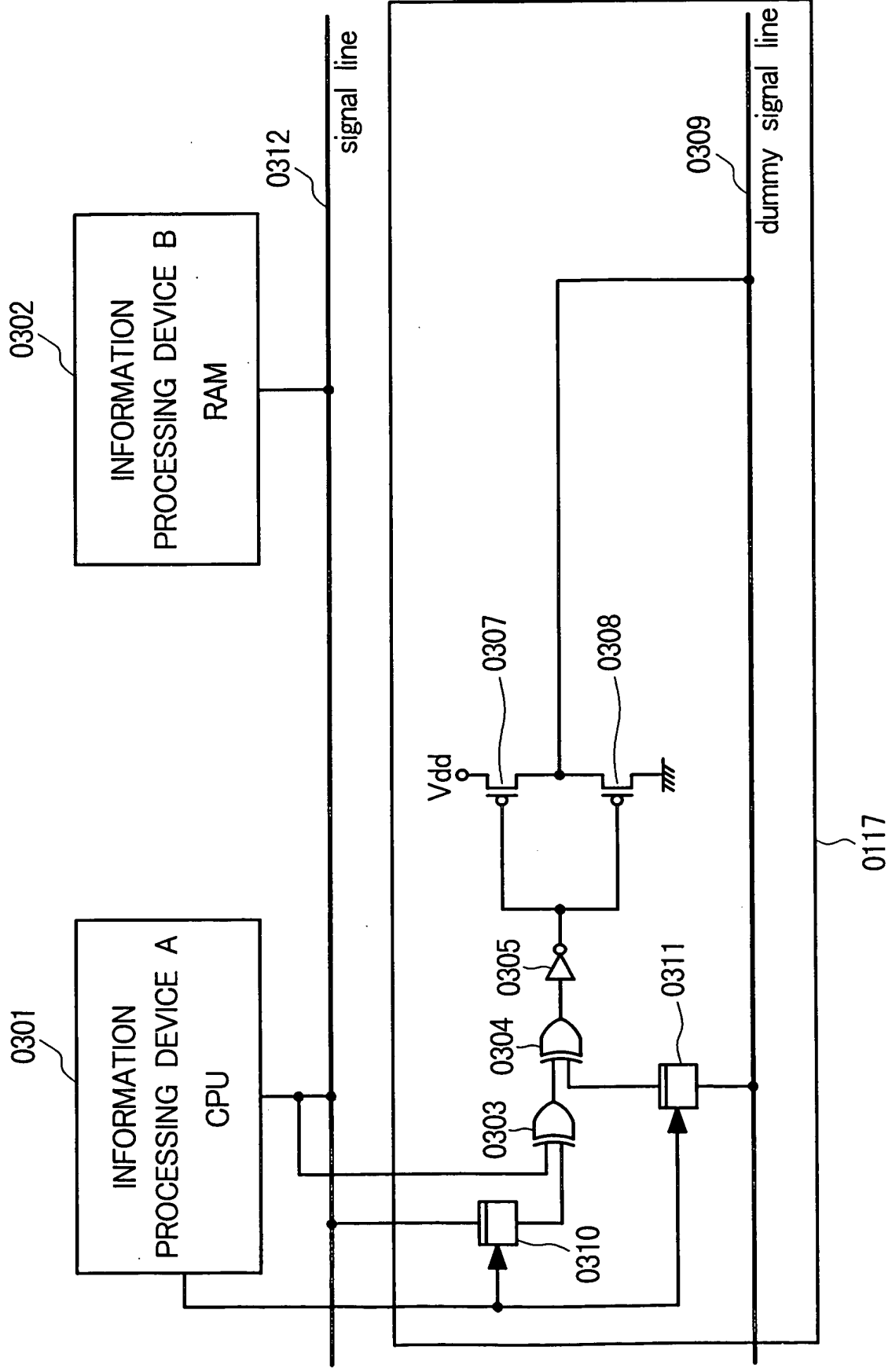


FIG.11

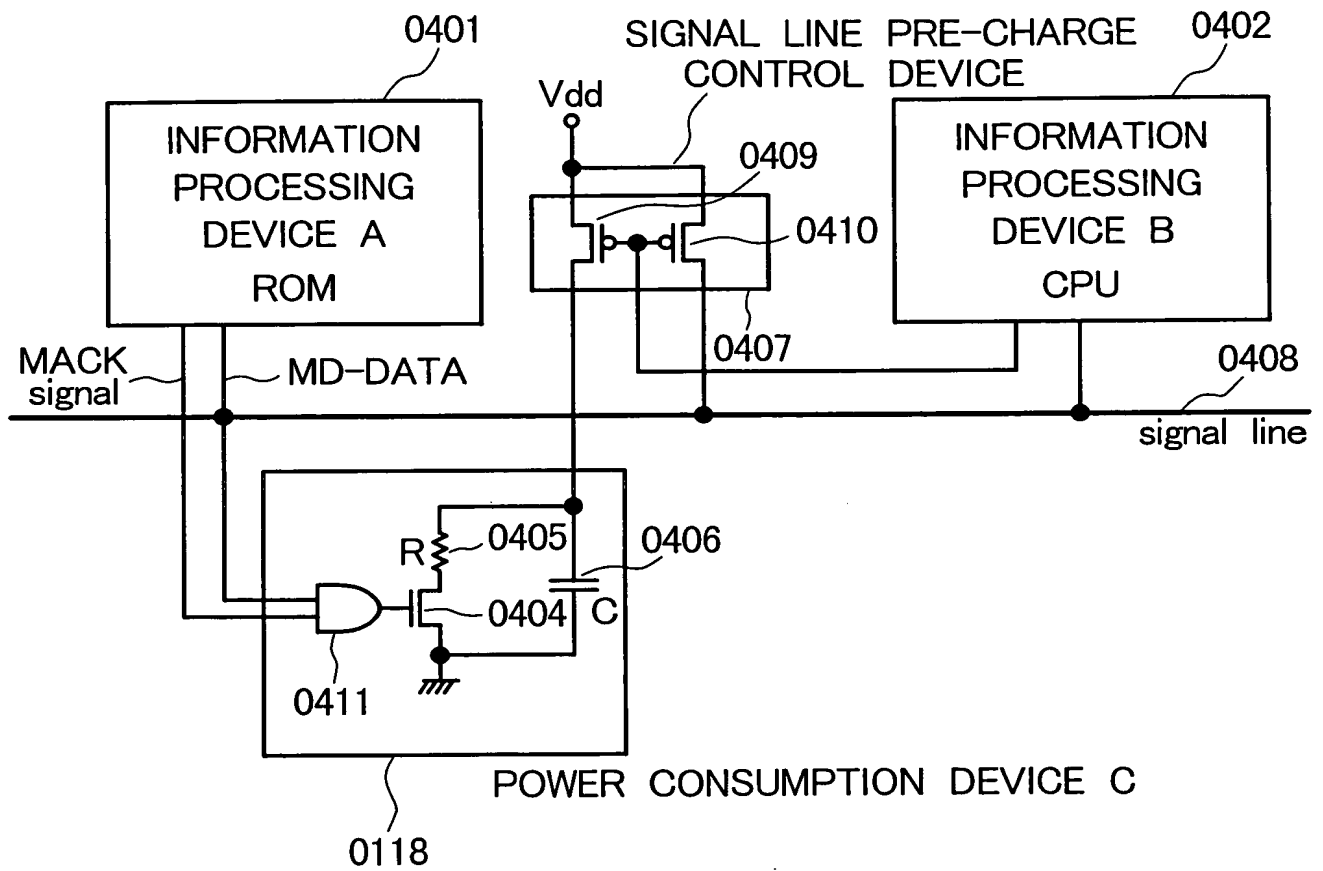


FIG.12

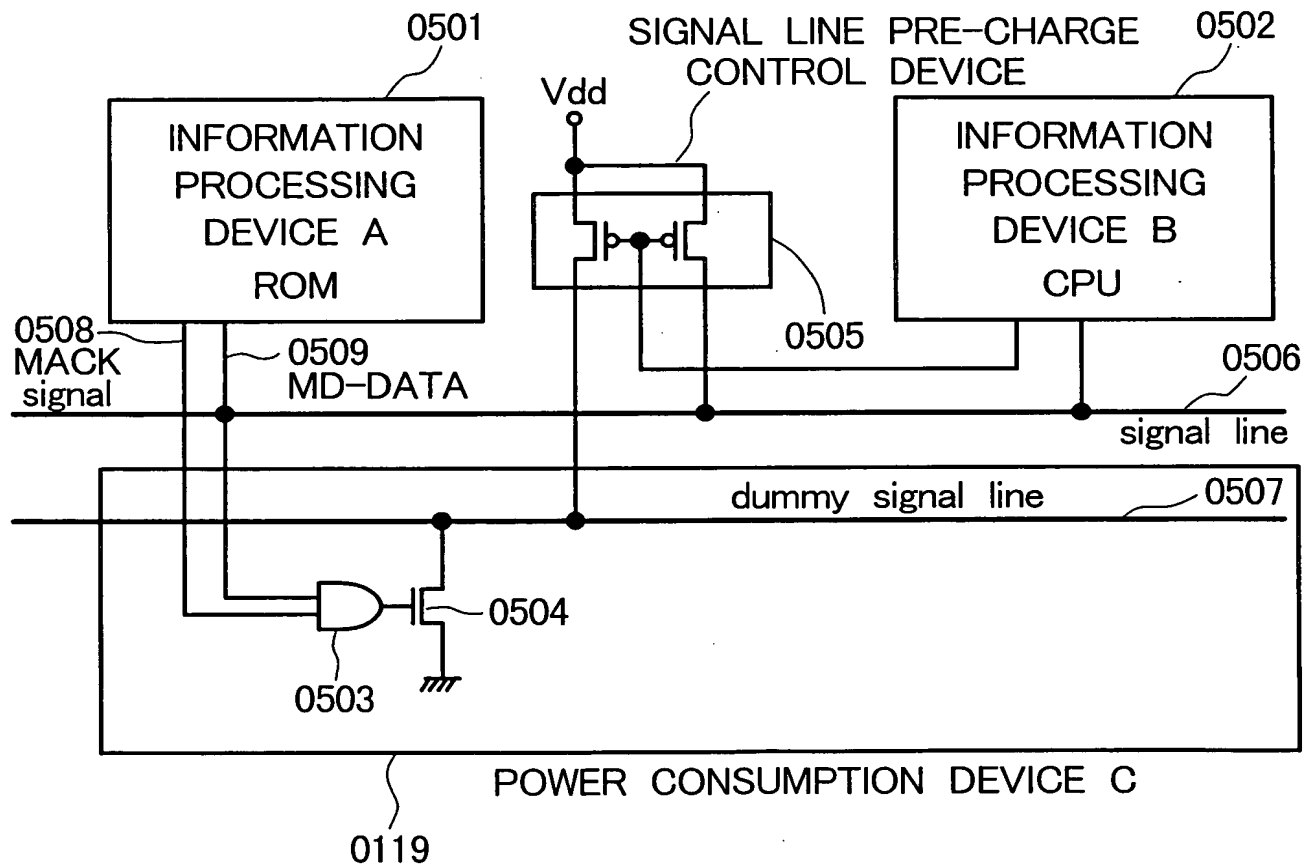


FIG.13

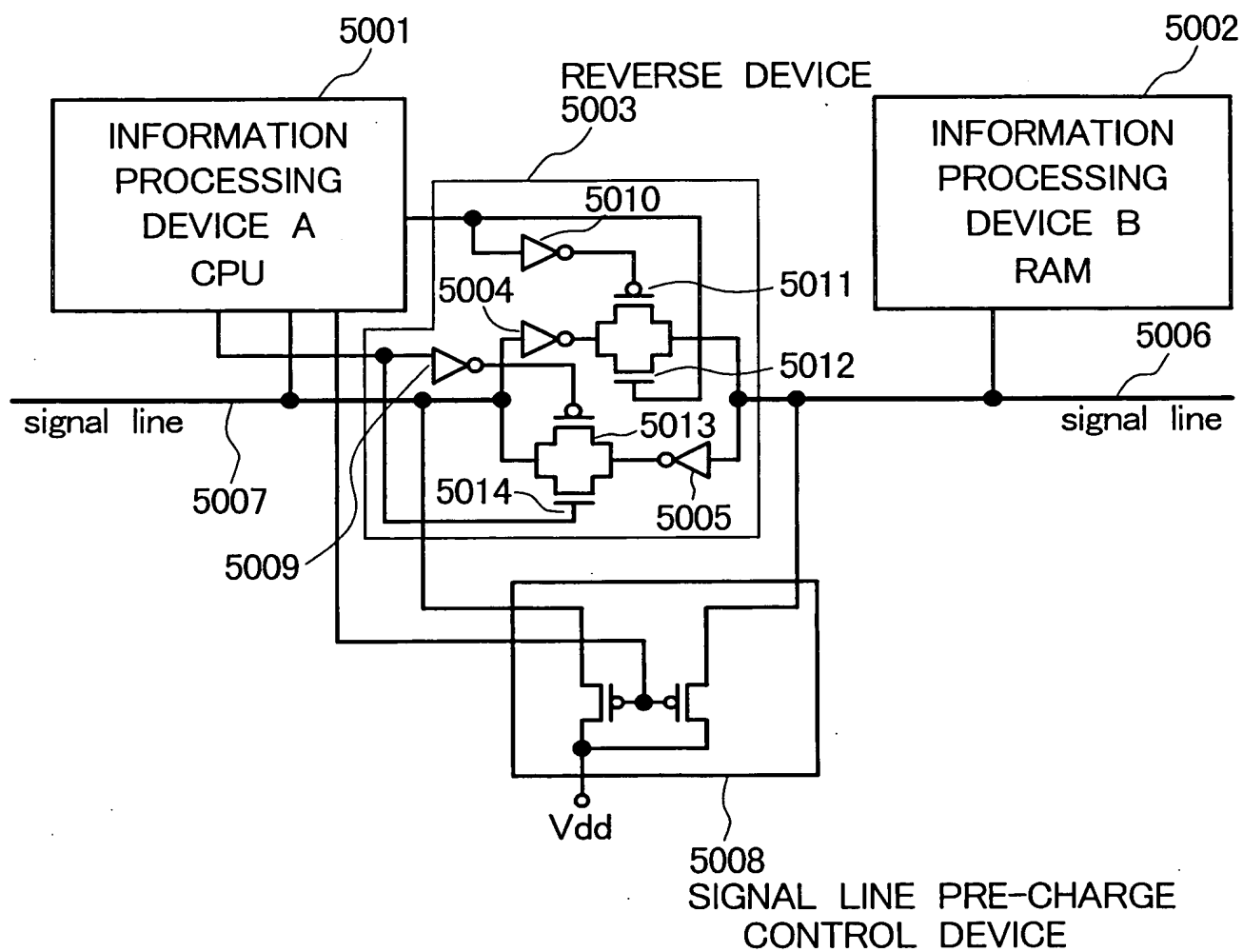


FIG.14

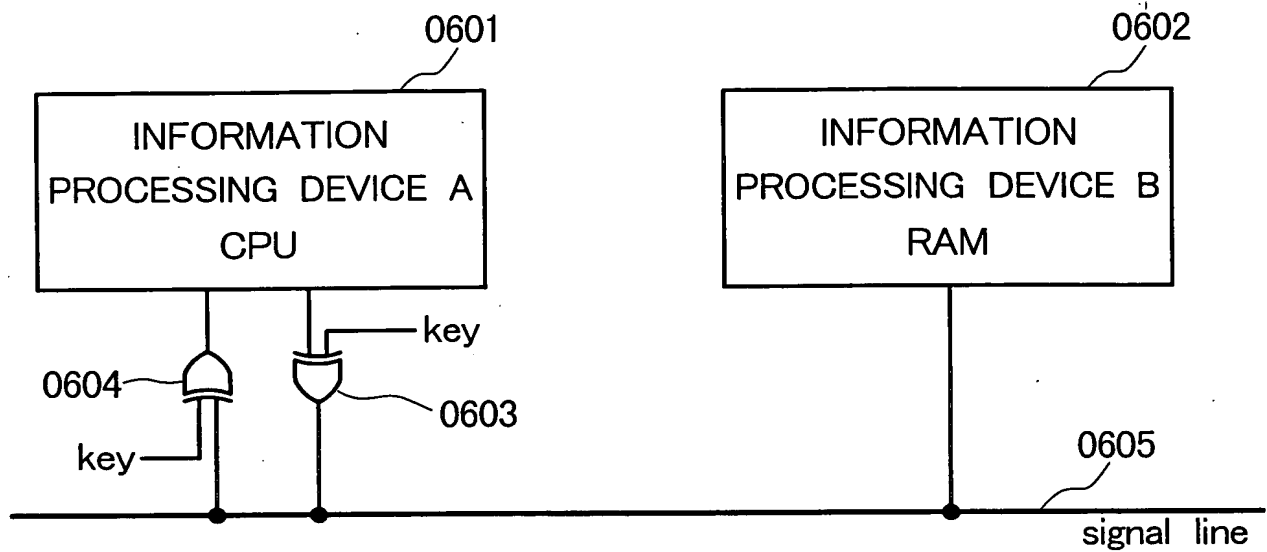


FIG.15

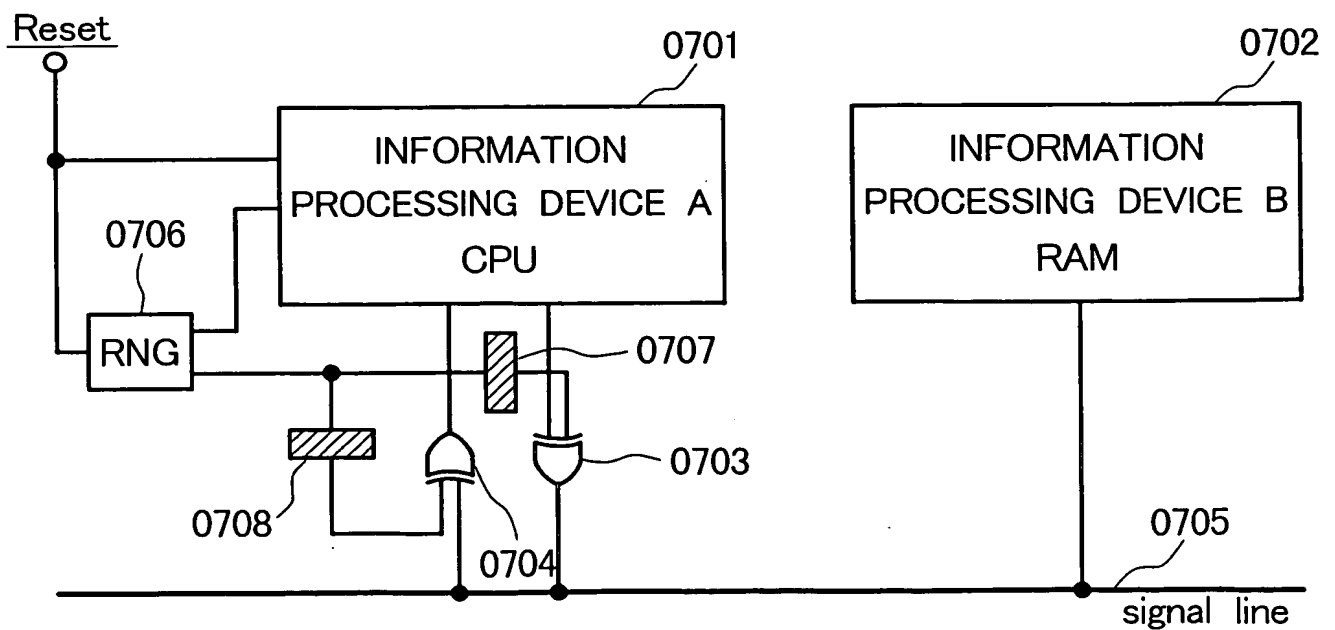


FIG.16

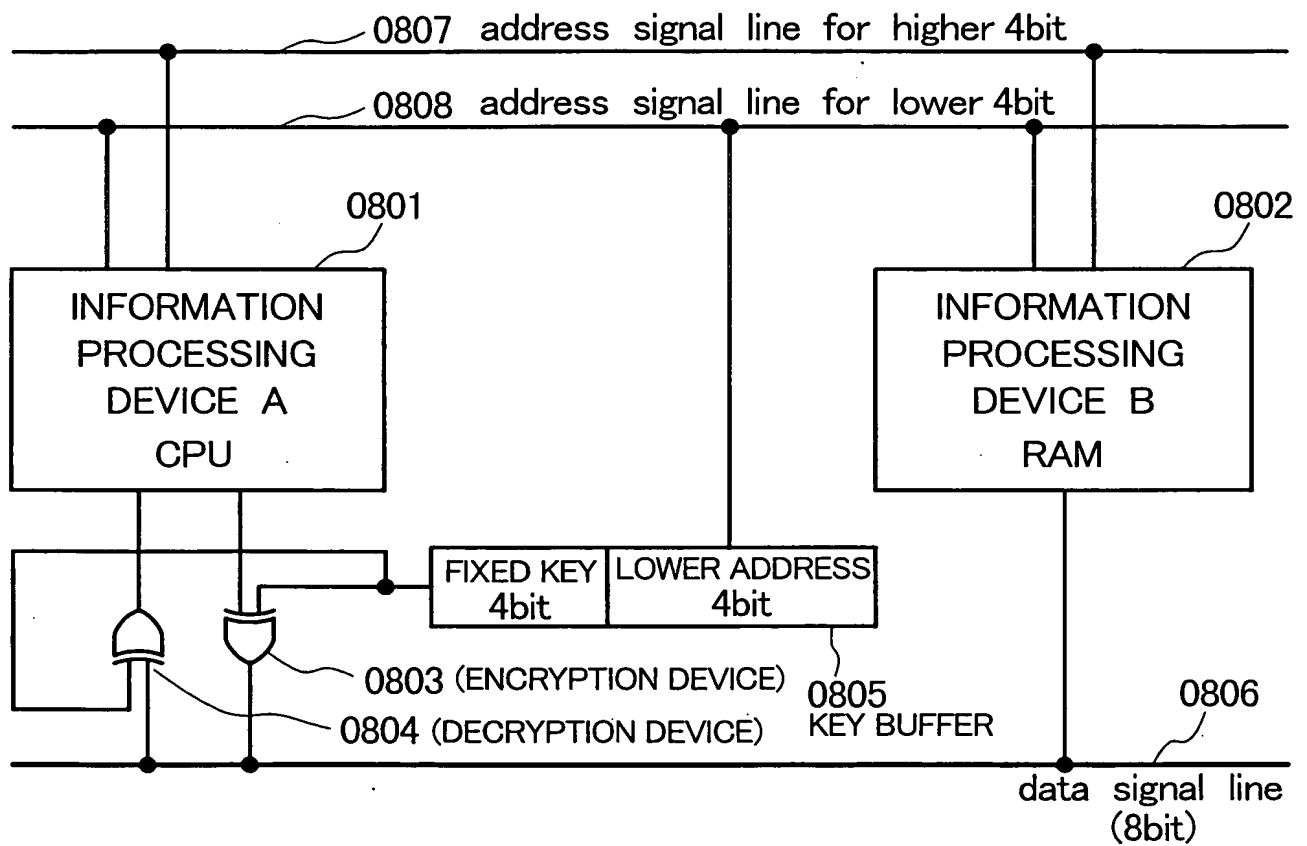


FIG.17

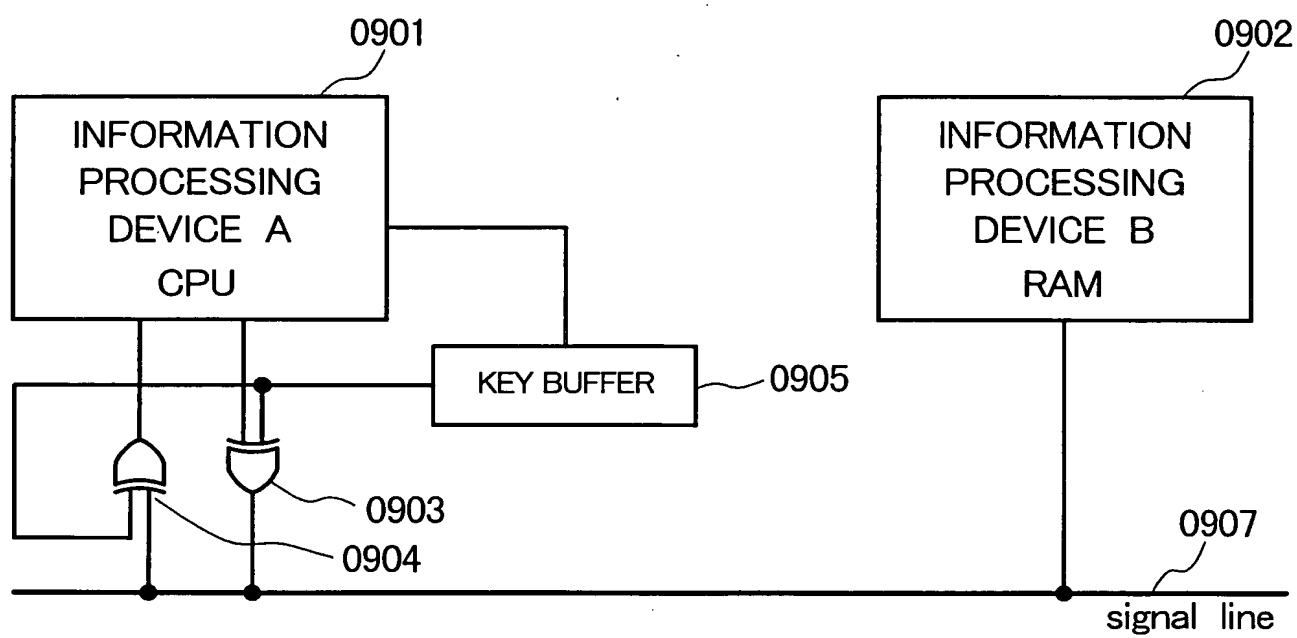


FIG.18

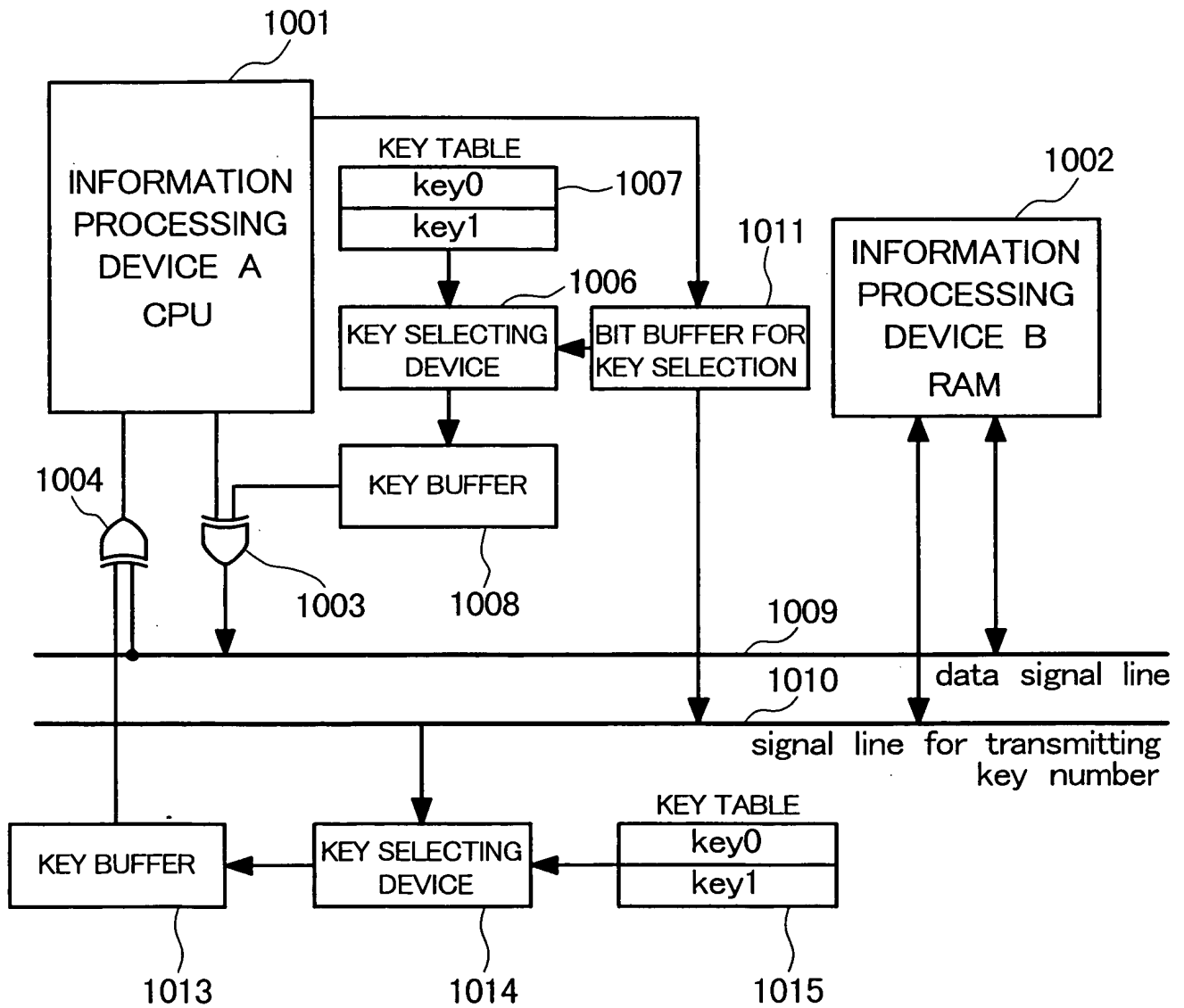


FIG.19

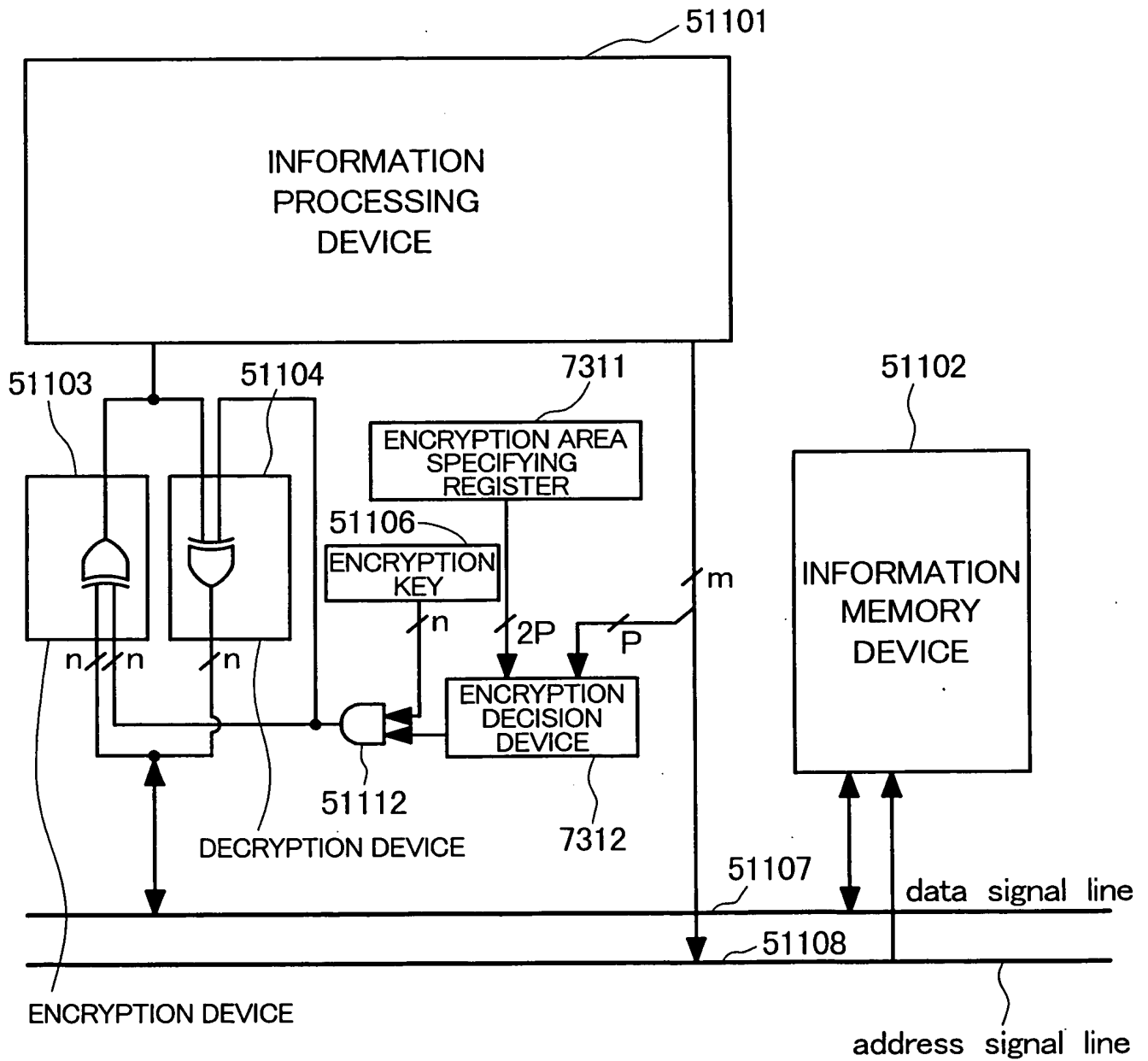


FIG.20

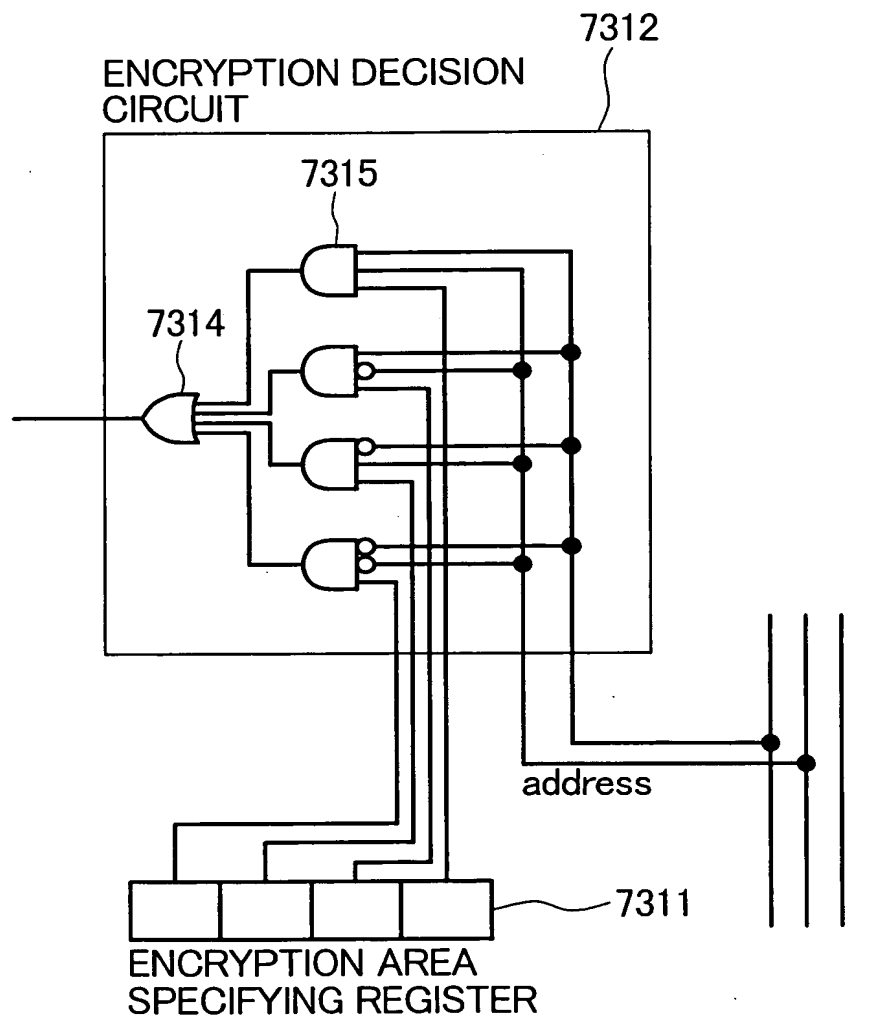


FIG.21

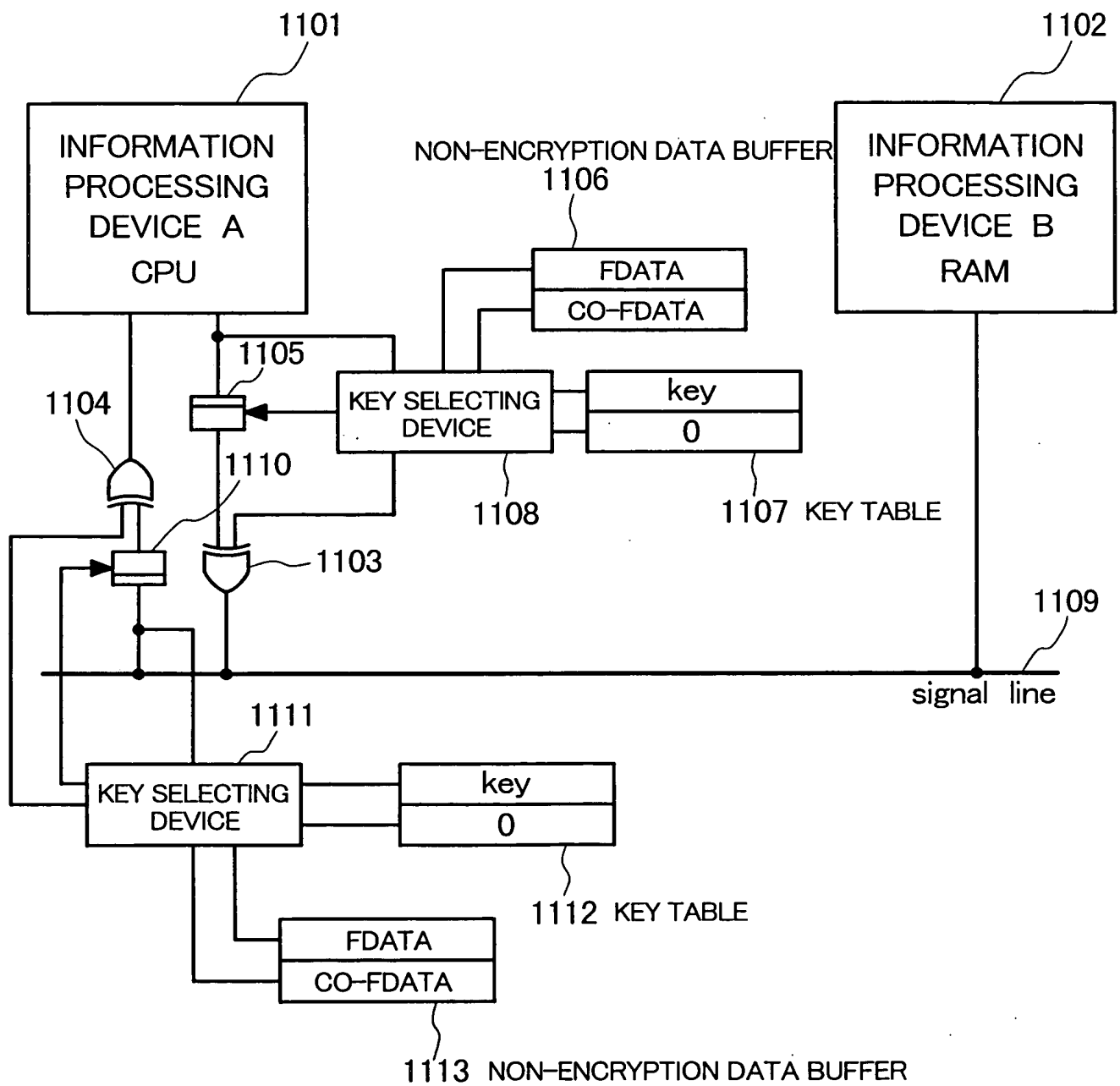


FIG.22

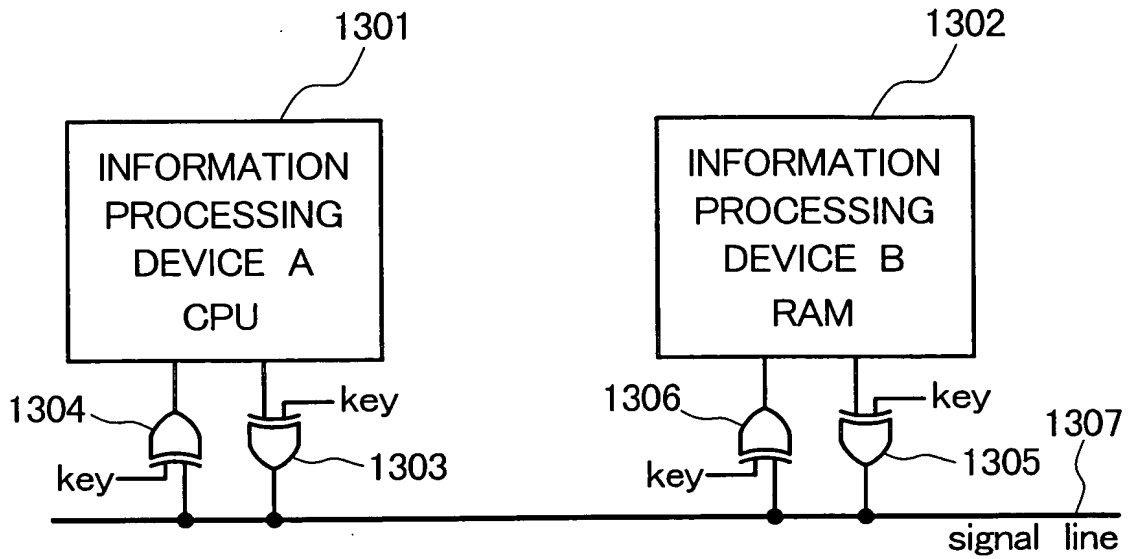


FIG.23

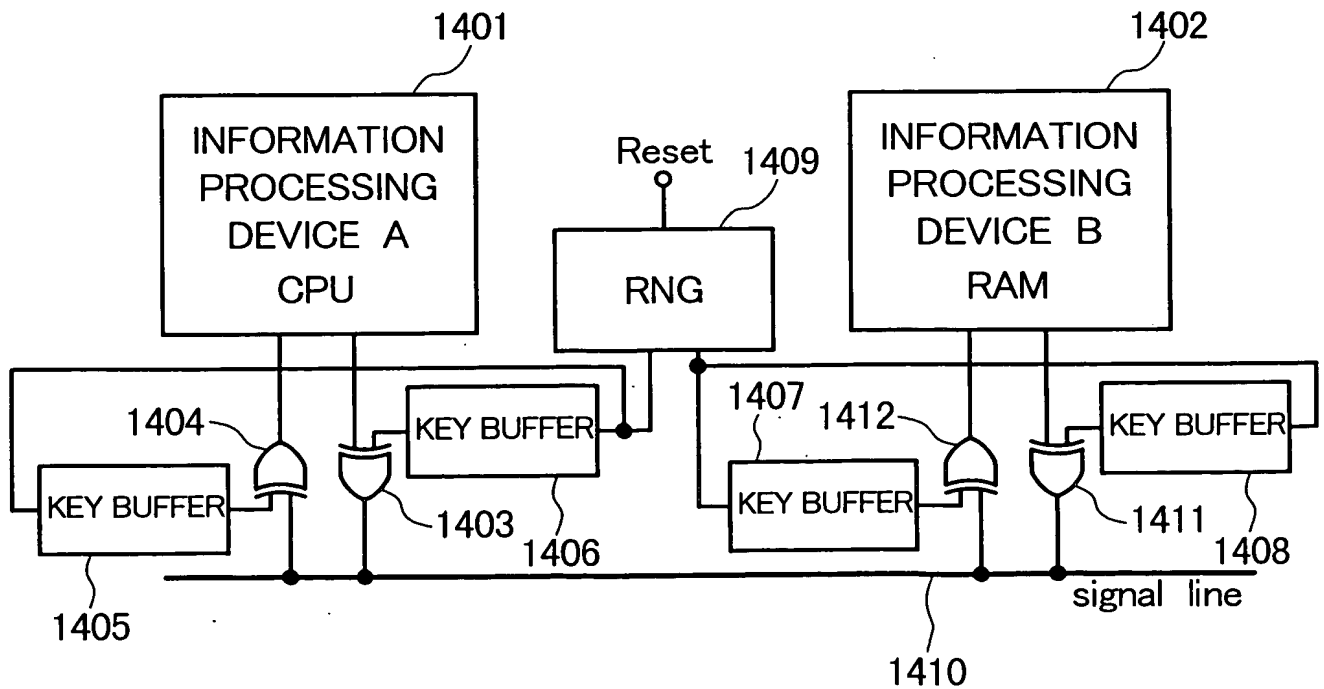


FIG.24

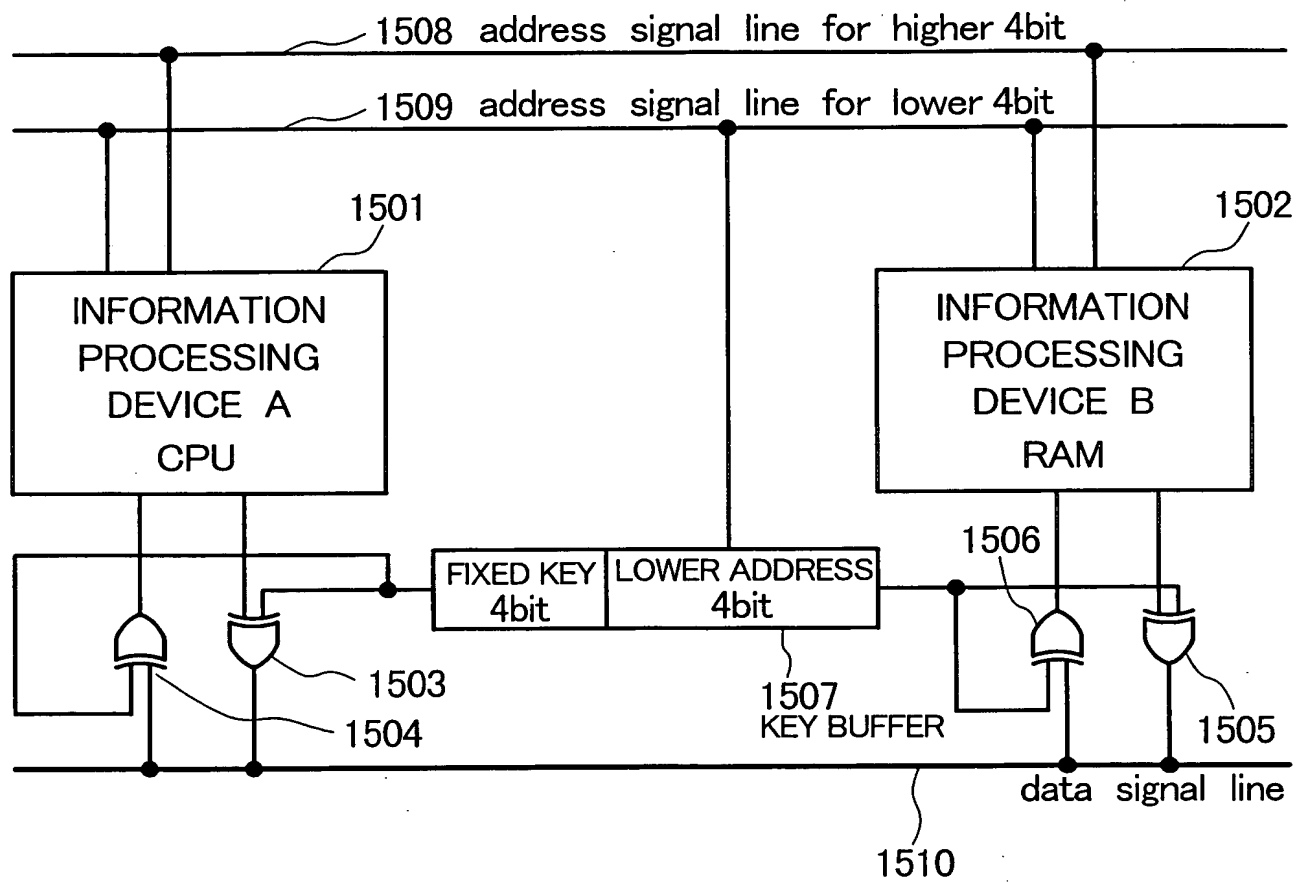


FIG.25

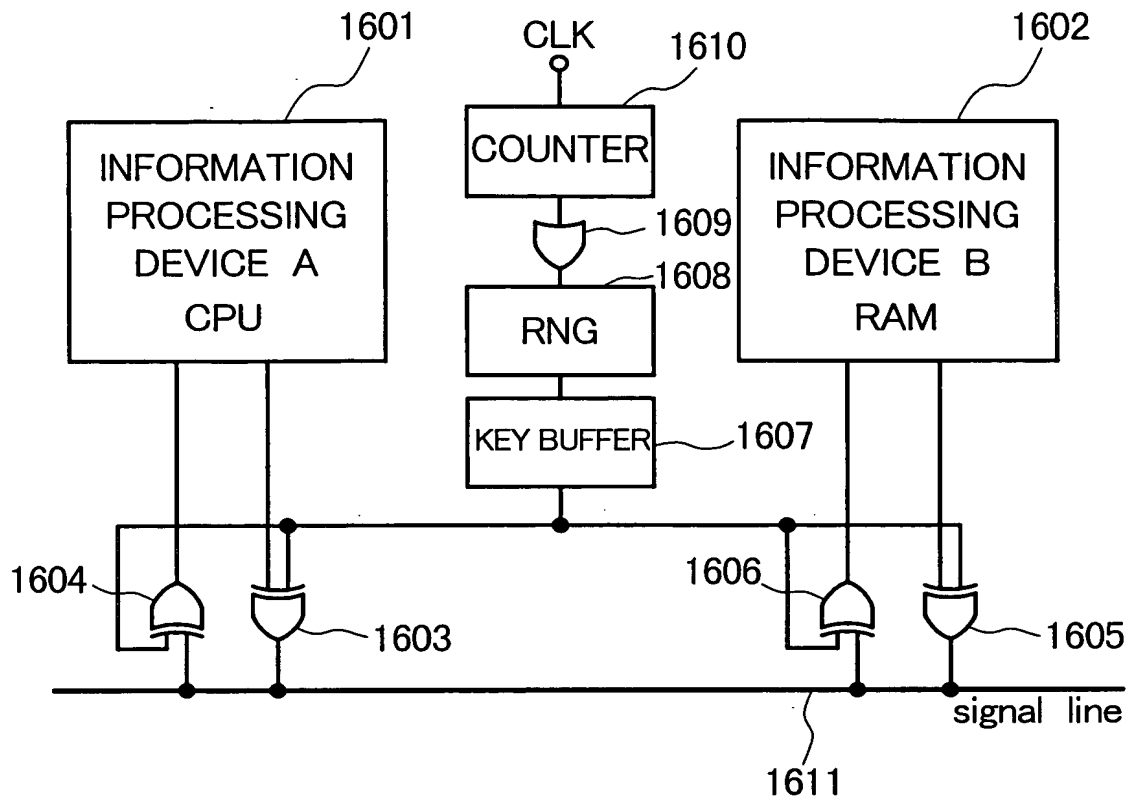


FIG.26

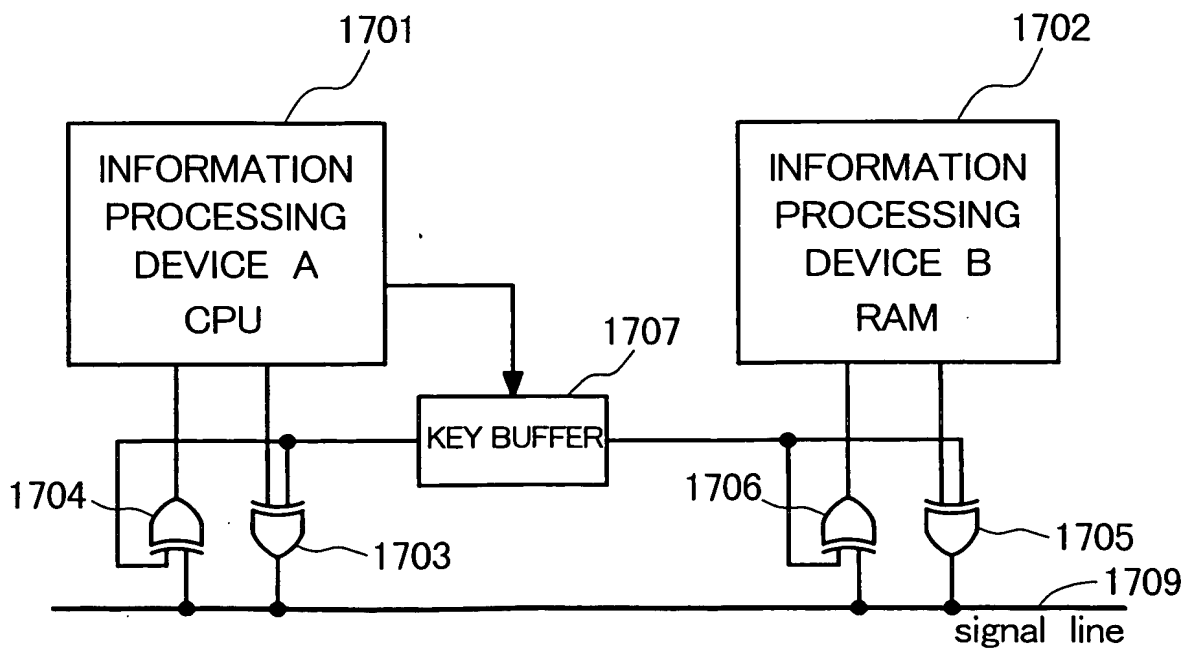


FIG.27

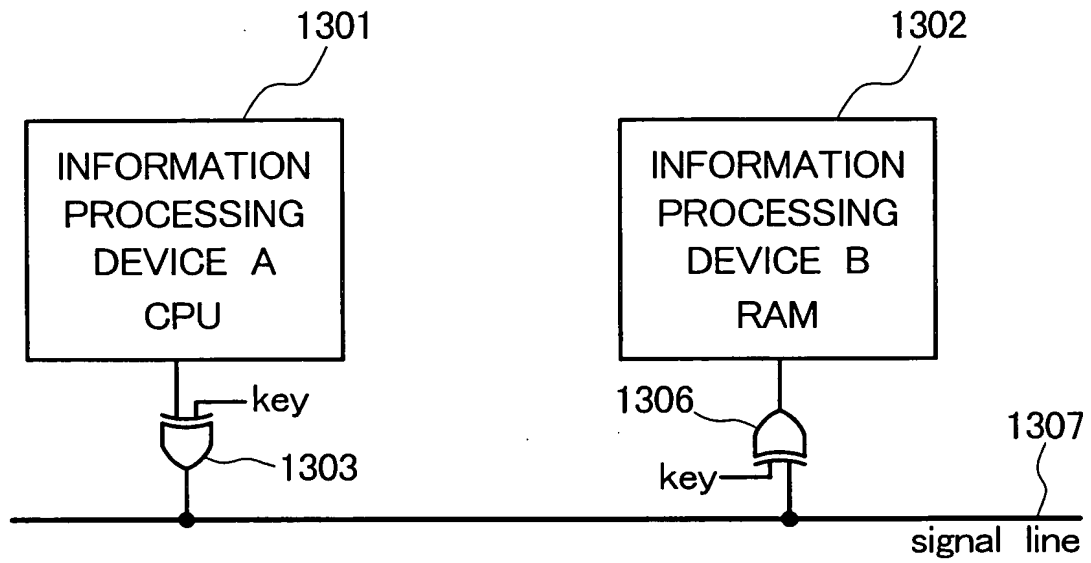


FIG.28

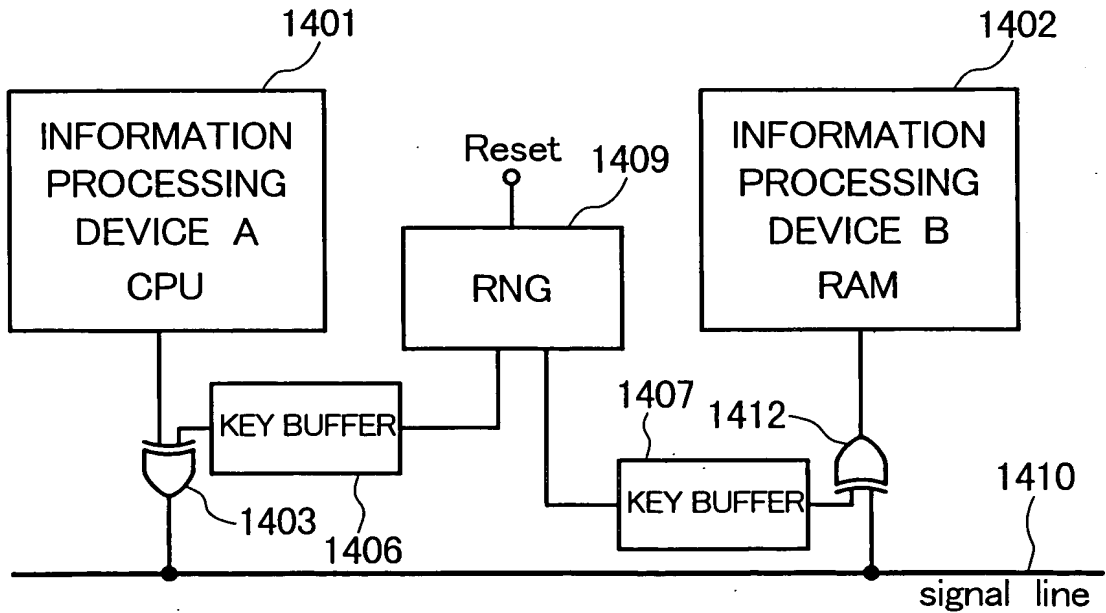


FIG.29

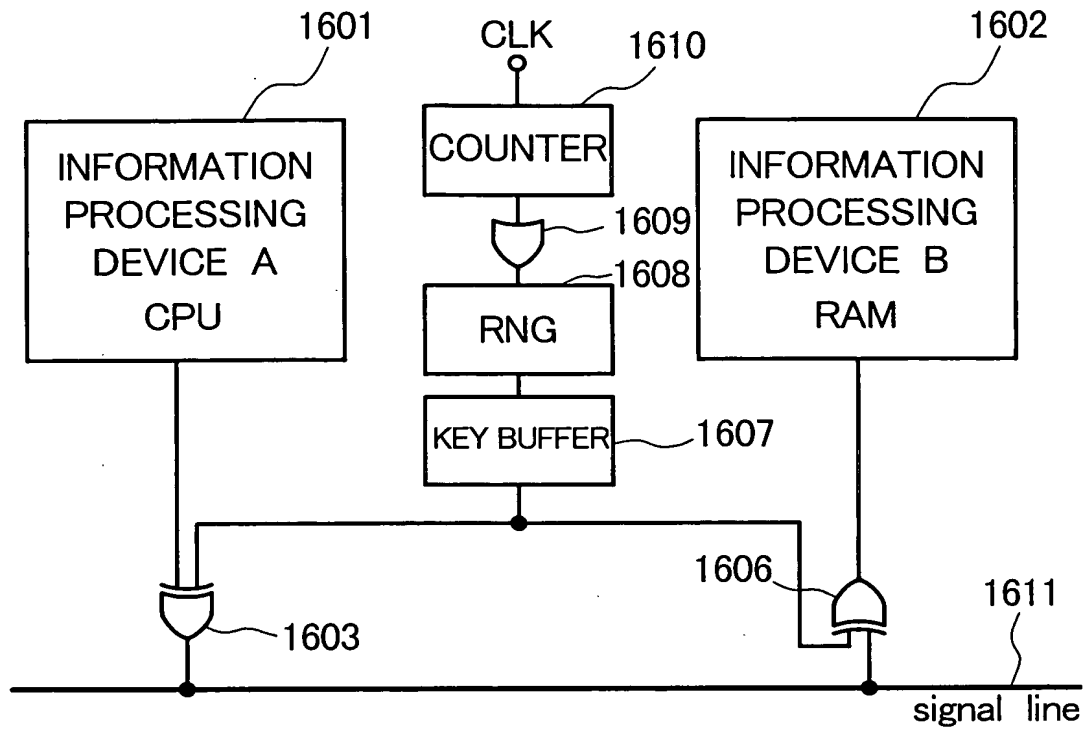


FIG.30

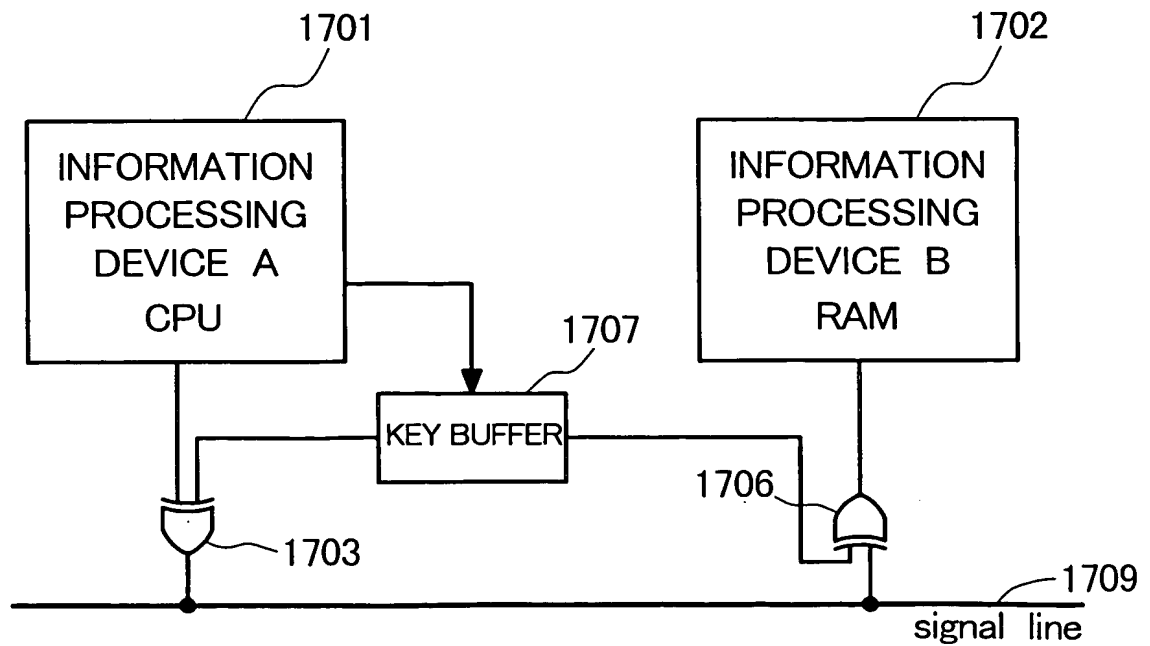


FIG.31

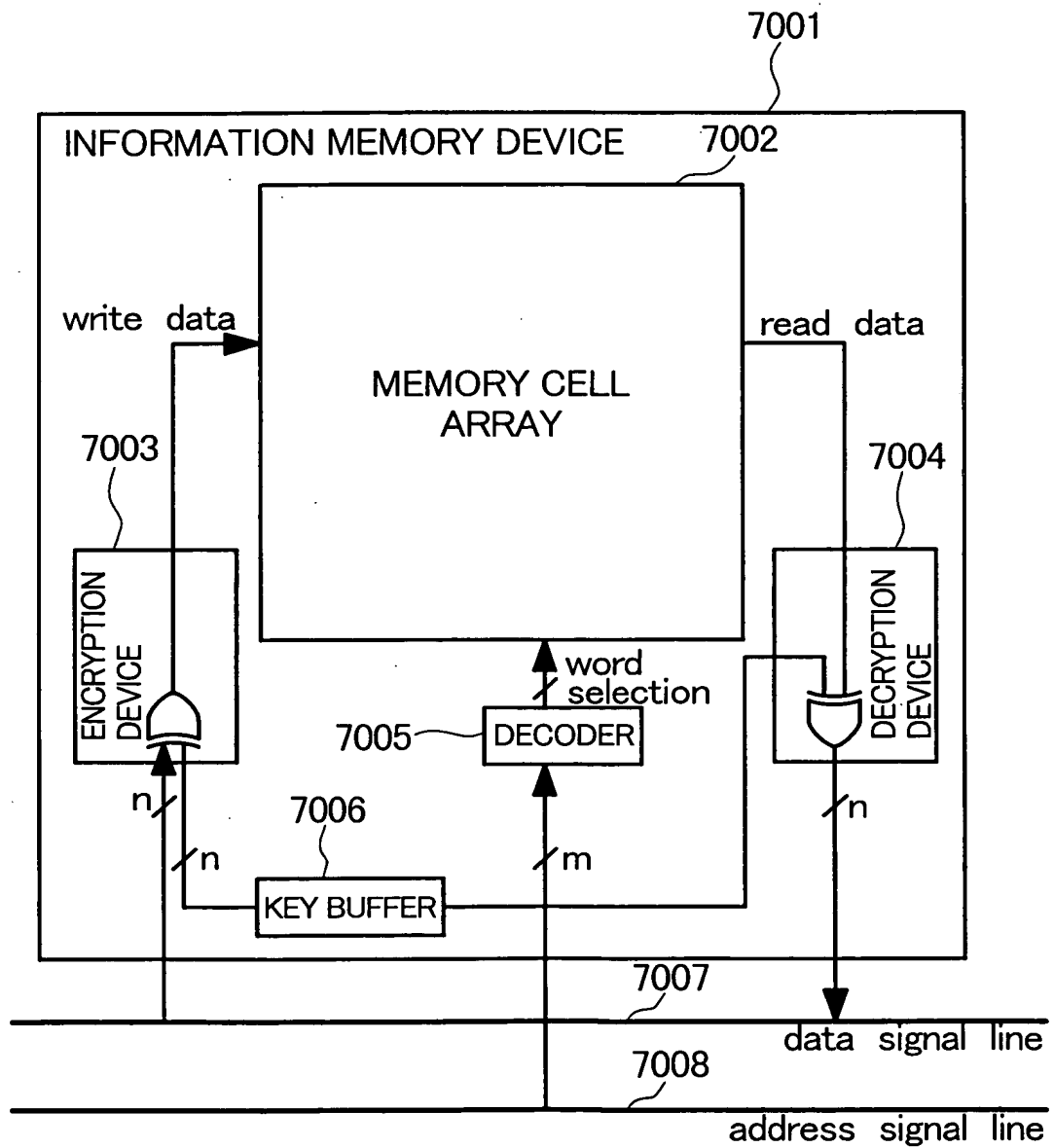


FIG.32

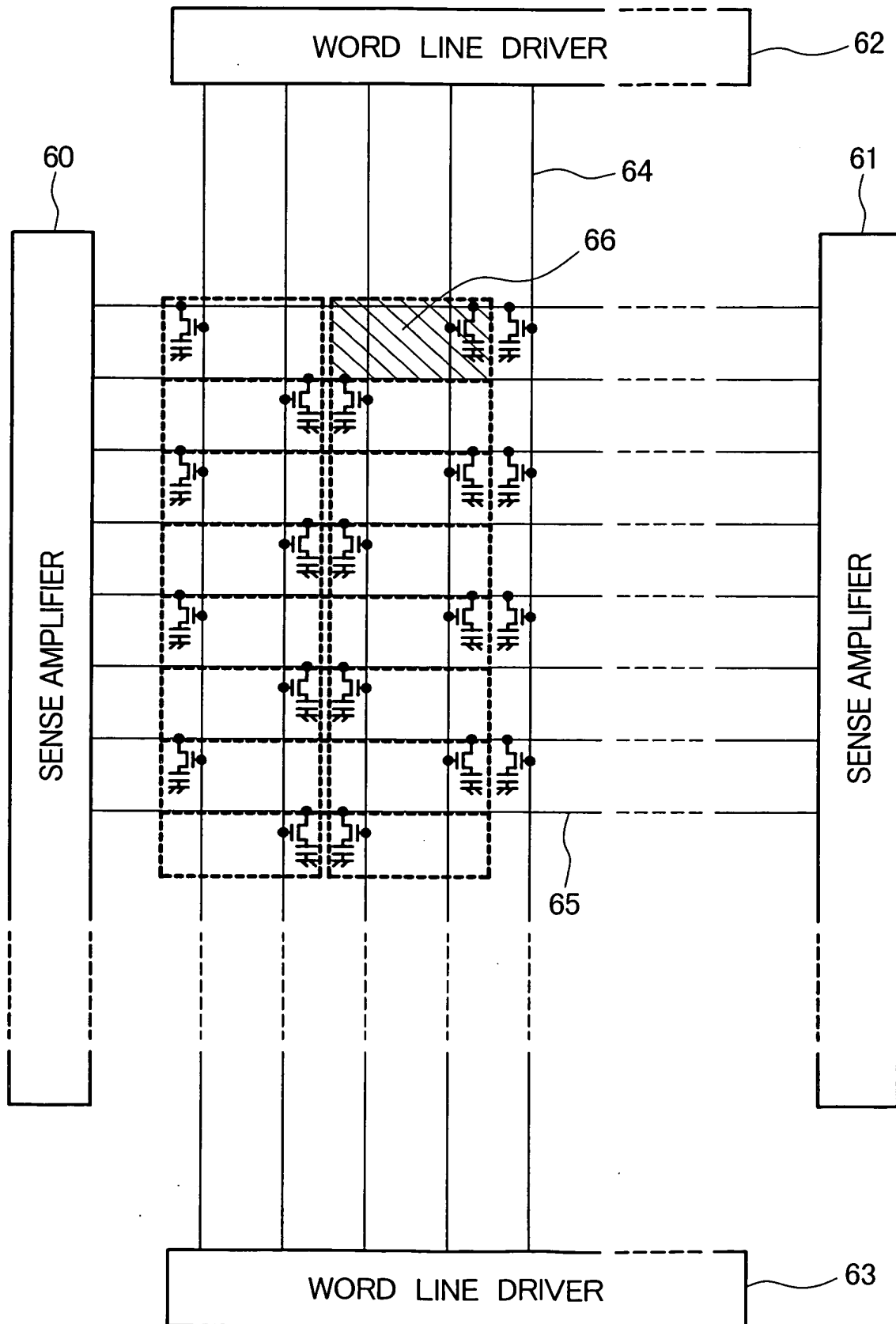


FIG.33

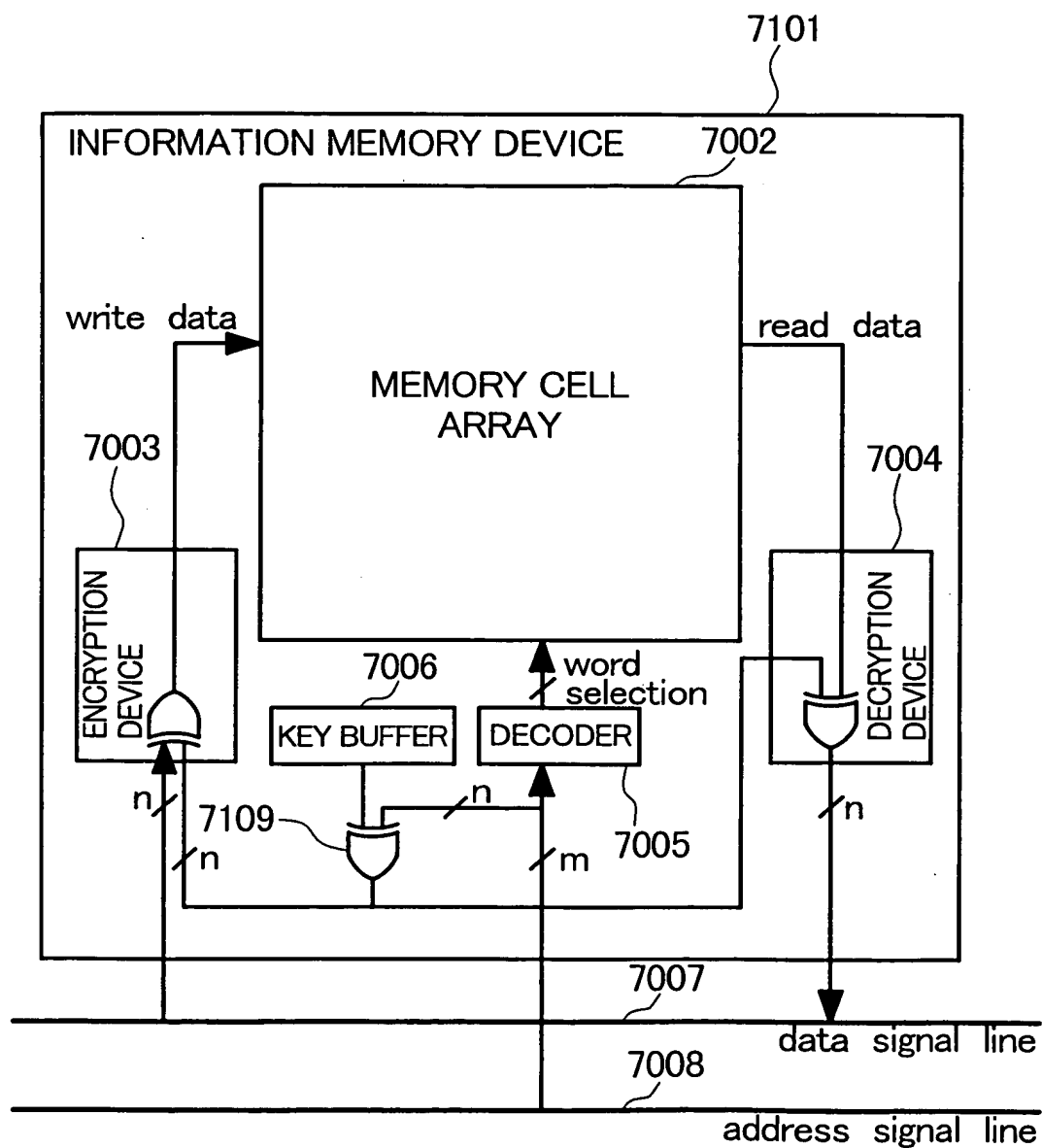


FIG.34

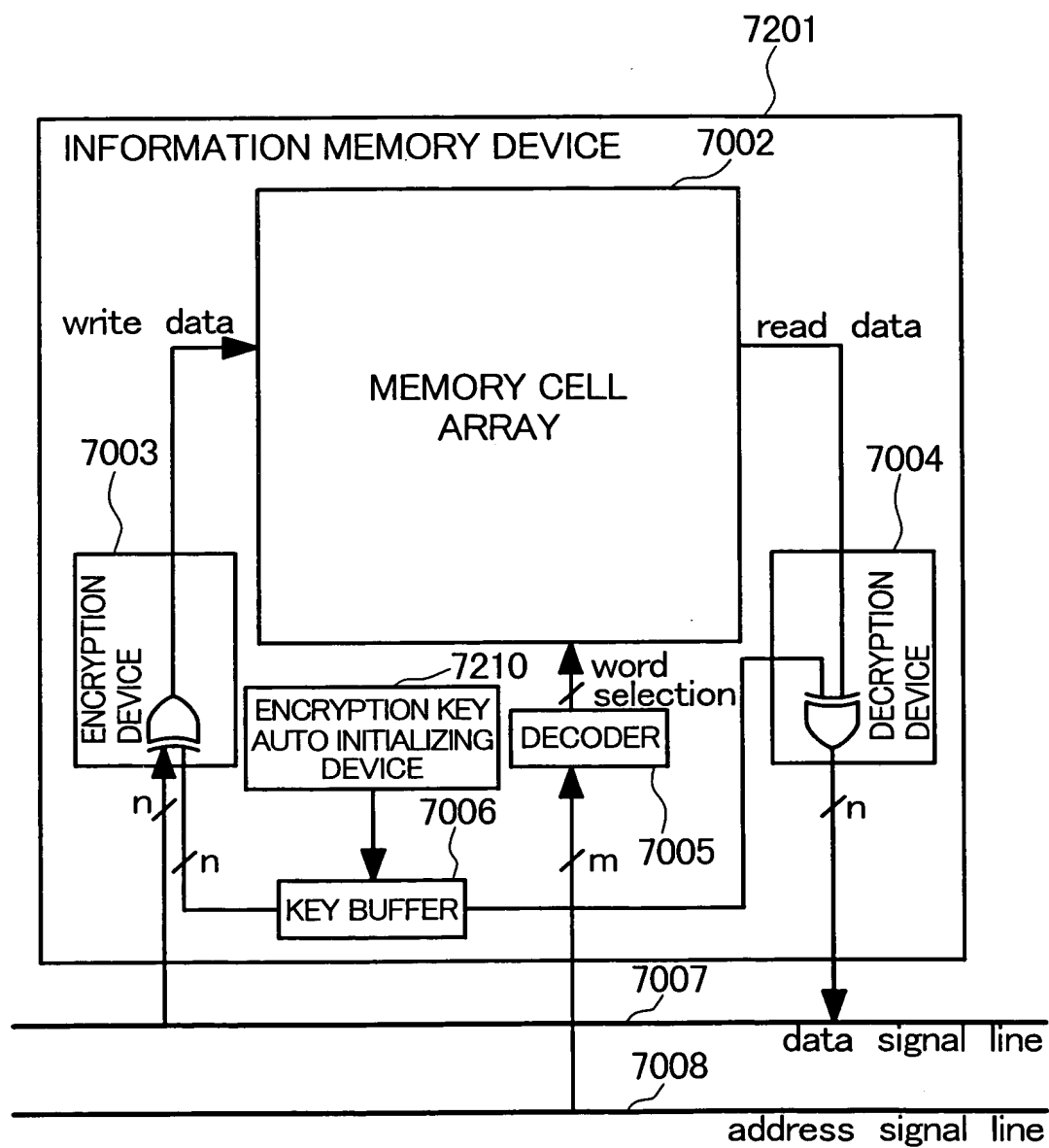


FIG.35

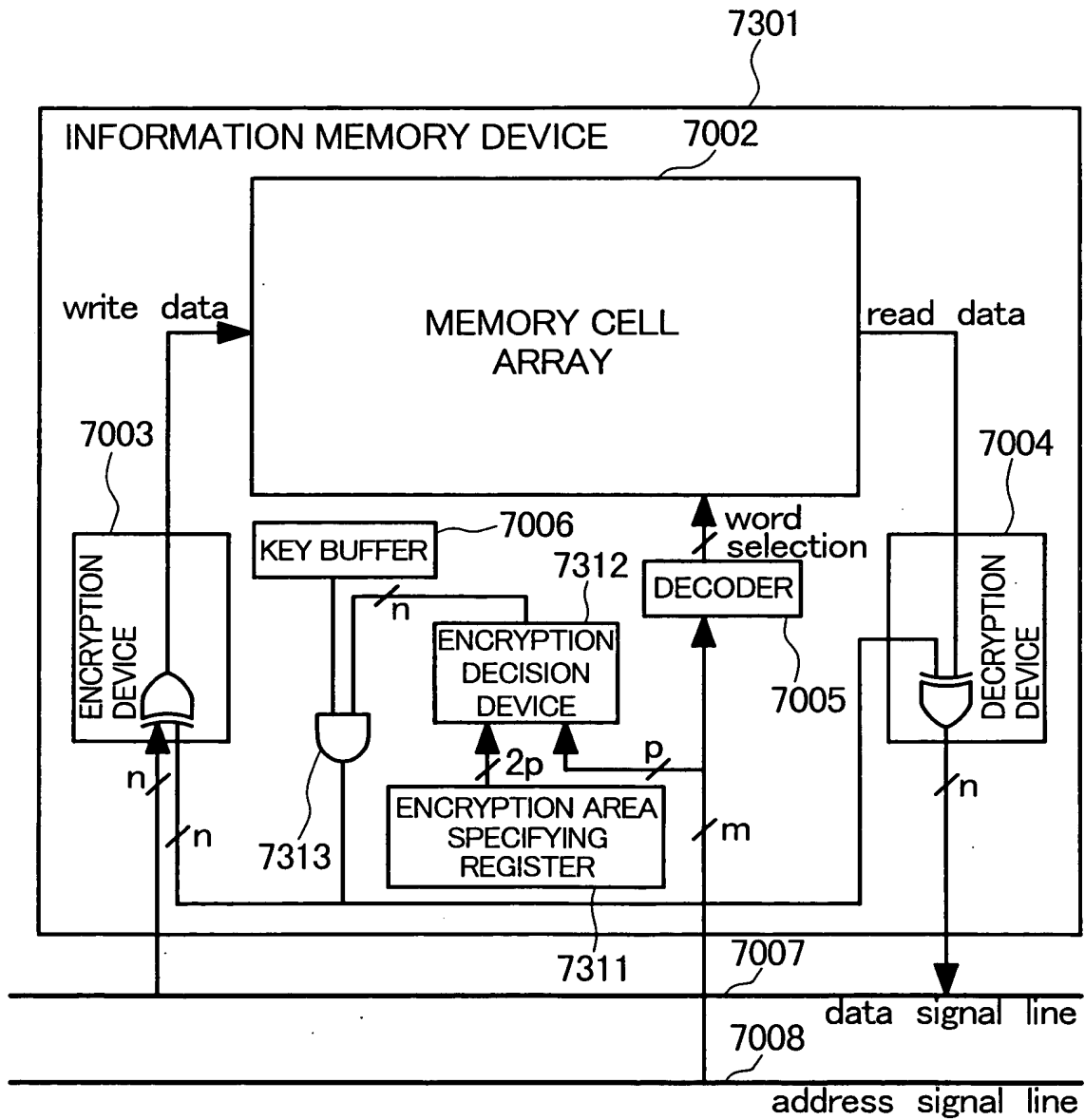


FIG.36

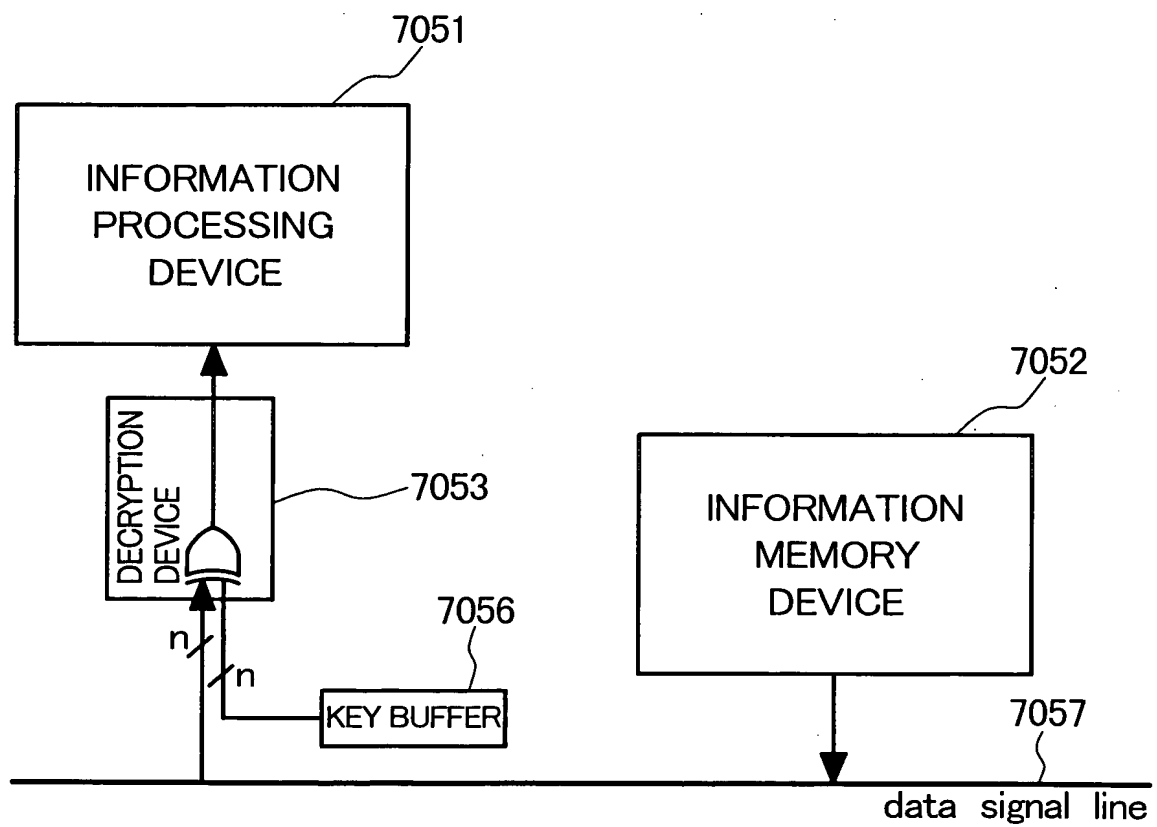


FIG.37

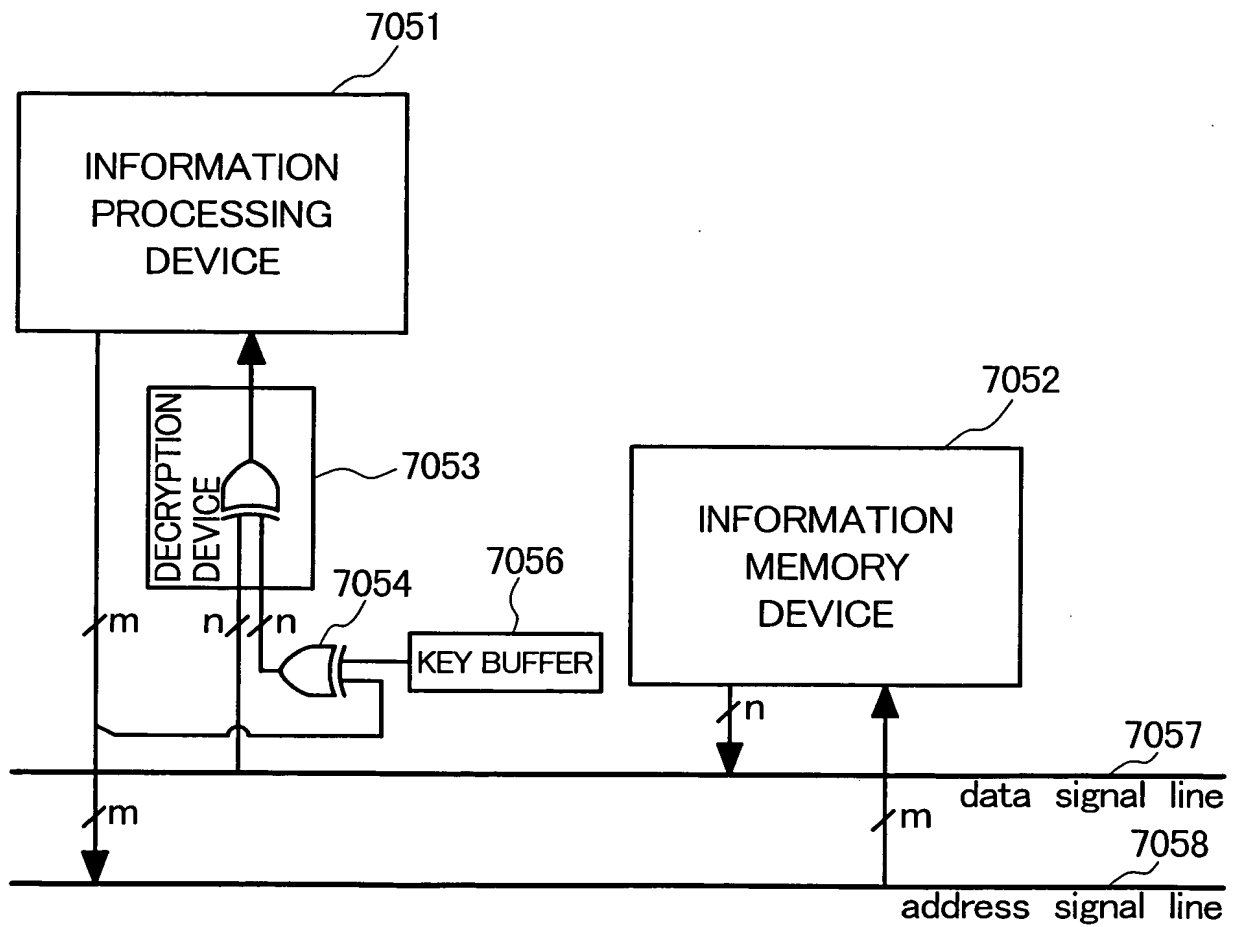


FIG.38

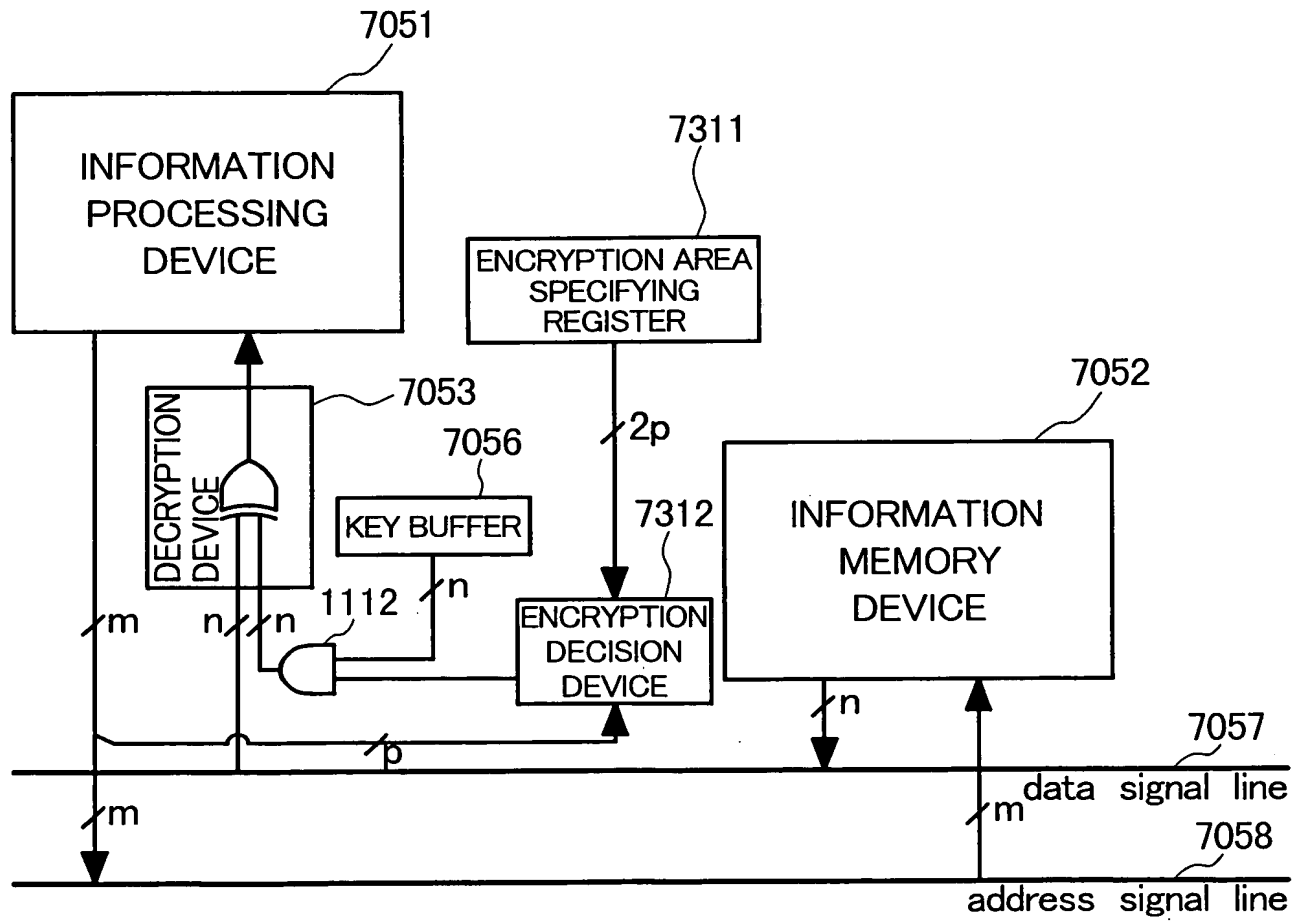


FIG.39

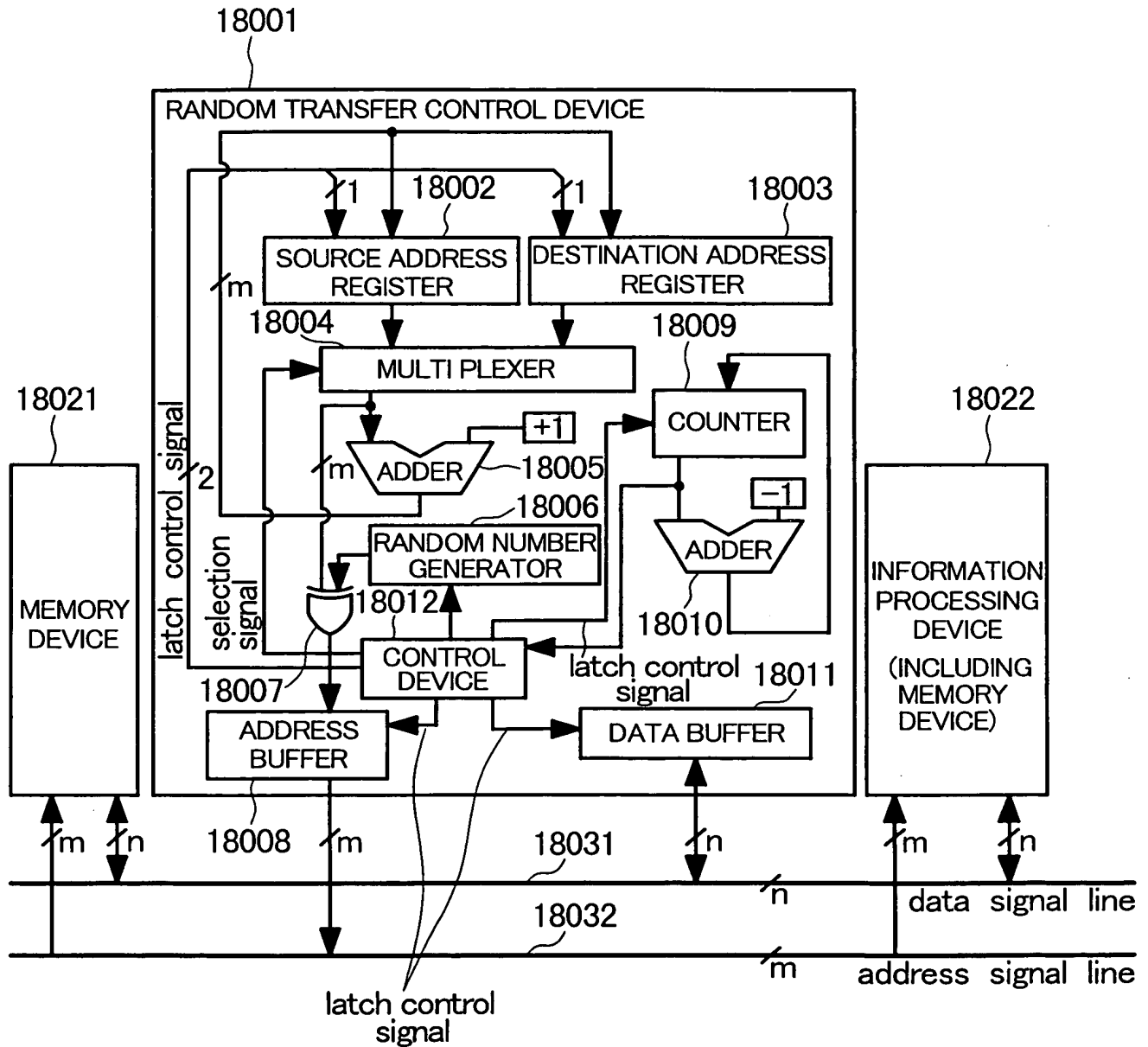


FIG.40

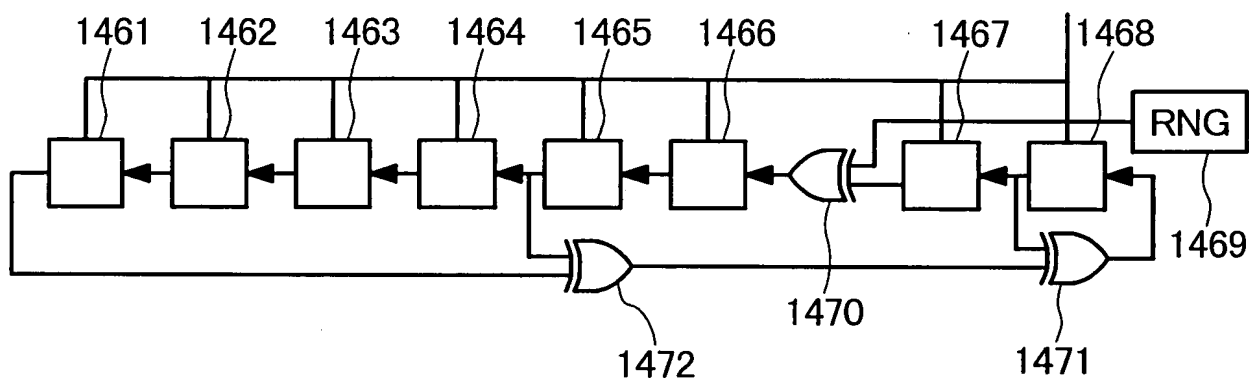


Table 1

PBD	DATA	CDD	Output for charging and discharging device in this invention
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Table 2

X	Y	X ExOR Y
0	0	0
1	0	1
0	1	1
1	1	0

Table 3

X	Not X
0	1
1	0

Table 4

Address	Data from CPU
F4	5D
F5	A0
F6	FE

Table 5

SKEYBIT (1 bit)	DATA (8 bit)
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